

Voltage Quality Analysis using Dynamic Voltage Restorer Based on Non-Linear Control Algorithms

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Abstract

The power quality of the electrical supply system has been impacted by the increase in non-linear loads and renewable energy sources such as the solar and the wind power integrated into the grid. The poor power quality results in equipment damage, system shutdown, and data loss, leading to lower operational efficiency and higher maintenance costs. The voltage sag, voltage swell, voltage flicker and voltage harmonic distortions are the most common and severe issues. The dynamic voltage restorer is the most effective solution for these voltage quality problems, which injects necessary voltage levels at the time of faults in order to maintain the load side voltage within specified boundaries. The appropriate control technique should be adopted for the generation of firing pulses for power electronic switches used to construct this device. The classical sliding mode control has the disadvantage of taking a long time to minimize errors. The main objective of this paper is to improve the accuracy and durability the conventional algorithm by adding nonlinear quantity, resulting in the fast terminal sliding mode controller. Furthermore, the artificial neural network is combined with proposed methodology to improve performance of double feeder power system for nonlinear load conditions. The system is modeled and simulated in a MATLAB/Simulink environment with a proportional integral controller optimized by particle swarm optimization, genetic algorithm and mind blast algorithm followed by non-linear controllers. The faults are simulated to mimic voltage sags A, E and B with different load conditions like linear, dynamic and non-linear. The power quality indices like total harmonic distortion, harmonic compensation ratio, sag score and voltage sag lost energy index are considered for assessment of compensation percentage. It is observed that Sag Score is improved by 80% thus increasing voltage sag lost energy index to more than 95%. Therefore, quantitative data demonstrate the efficacy of the proposed method in mitigating voltage sag while simultaneously reducing grid voltage imbalance and distortion, irrespective of the fault type.

Keywords- Power quality, Fault conditions, Dynamic voltage restorer, Sliding mode control, Artificial neural network.

Abbreviations

DC	Direct Current
PQ	Power Quality
DVR	Dynamic Voltage Restorer
VSI	Voltage Source Inverter
SMC	Sliding Mode Control
TSMC	Terminal Sliding Mode Control
FTSMC	Fast Terminal Sliding Mode Control
PI	Proportional-Integral
PSO	Particle Swarm Optimization
GA	Genetic Algorithm
MBA	Mind Blast Algorithm
ANN	Artificial Neural Network
ANFIS	Adaptive Neuro-Fuzzy Inference System

MLP	Multilayer Perceptron
FLC	Fuzzy Logic Controller
LMS	Least Mean Square
<i>d</i> -axis	Direct Axis
<i>q</i> -axis	Quadrature Axis
THD	Total Harmonic Distortion
THDV	Voltage Total Harmonic Distortion
HCR	Harmonic Compensation Ratio
SS	Sag Score
VSLEI	Voltage Sag Lost Energy Index
SRFT	Synchronous Reference Frame Theory
RMS	Root Mean Square
p.u.	Per Unit
p.f.	Power Factor
LG	Line to Ground
LLG	Double Line to Ground
LLLG	Triple Line to Ground
AC	Alternating Current
CT	Coupling Transformer
PLL	Phase-Locked Loop
RVG	Reference Voltage Generator
IC	Inverter Controller
Vabc	Three phase sinusoidal line voltage
SRFT	Synchronous Reference Frame Theory
PWM	Pulse Width Modulation
IRPT	Instantaneous Reactive Power Theory

1. Introduction

Electricity is generated in power plants, but the use of non-linear devices and other problems in the supply system can lead to the degradation of Power Quality (PQ) which is threatening situation for consumers and industries. High-quality power as defined by IEEE 519 is necessary to ensure smooth manufacturing processes. However, this can only be achieved if disruptions in the supply chain are addressed. Many complaints related to power quality have been received, including voltage sag, which is particularly problematic as it can cause other issues. Sensitive loads are especially vulnerable to voltage fluctuations, which can lead to reduced efficiency and complications in machinery. The stability of the system is ultimately determined by the extent of the residual voltage rather than the frequency or duration of dips. The voltage drops can be caused by various factors such as faulty wiring, starting motors or turning on large transformers. These drops can result in financial losses and reduced productivity for businesses. For some customers with sensitive equipment, a voltage-correcting system may be the only viable option. There are various methods to mitigate voltage drops, such as using a voltage-source inverter connected to the power supply system and the sensitive load as a series connection. A Dynamic Voltage Restorer (DVR) is a common term for this type of device, rapidly restoring the load voltage to the level before the fault can help stabilize the system voltage. The DVR is an easy, versatile and efficient way to fix voltage drop problems. In order to restore the load voltage, any power outage or any other PQ issue will be minimized in milliseconds. As a basis for the design of a series of active filters, the authors, Battista and Mantz (2000) suggest a variable structure concept. The current measured from the harmonic source is the basis for the control method, which is based on the Instantaneous Reactive Power Theory (IRPT). This is discovered that an excessive rating of the converter is required to compensate for the current harmonics induced by quickly changing loads. The current control methods used to design the DVR, such as feed-forward control & Proportional Integral (PI) feedback control, all use the Sliding Mode Control (SMC) scheme, encapsulated in Ruilin and Yuegen (2005). The controller's inaccurate estimation of the inductance impact brought on by harmonic current is a known shortcoming, resulting in subpar compensation and voltage regulation. Utilizing a DVR in sliding mode to keep the load voltage near the source voltage, a control for

minimal energy injection is offered (Piatek, 2005). Only linear loads are considered by the system. The SMC is realized in the design of a single-phase DVR by Errabelli et al. (2006), at the load end the voltage is regulated to satisfaction but transients are visible in the waveform of the corrected load voltage. Authors Kumar and Chowdary (2008) elaborated the load voltage is the basis for the control method. However, not all voltage-related power quality issues are accounted for in the demonstrated findings, despite claims that DVR can do a lot. Topology for a synchronous reference frame-based phase-locked loop with a sliding mode-controlled DVR is presented by Pires et al. (2011). The SMC approach was used to identify the phase and frequency of power system voltages quickly and reliably. The authors' results are insufficient to validate the usefulness of the projected controller. To provide a standard oscillating signal, the SMC in conjunction with a PI method for DVR is proposed by Mahalakshmi et al. (2013). Using a Direct Current (DC) link capacitor and a wind energy conversion technology based on permanent magnet synchronous generators, DVR can store and use DC energy. The resulting simulation findings are solely useful for preventing voltage sag and do not provide any insight into other power quality issues. To diminish voltage amplitude variations at the load location, a twelve-switch and three-phase voltage source converter is employed (Biricik et al., 2015) with a double-band hysteresis control and a sliding mode control method (Biricik and Komurcugil, 2016) as well as an adjustable notch filter (Biricik et al., 2019). The Writers Naidu et al. (2020), to handle voltage sag, swell, imbalance, and distortions, the GAVS-LMS algorithm was used to examine the performance of the DVR. In (Hasan et al., 2021), A DVR is controlled experimentally using a dual slope delta modulation approach, which has been shown to alleviate Voltage Sag issues in power systems. A single-phase DVR using a PLL with super twisting SMC and a Brockett oscillator was developed by authors in Biricik et al. (2021). To address voltage-related power quality issues, an optimized PI-tuning Sliding Mode Observer (SMO) has been implemented in a DVR (Naidu et al., 2020). Authors in Elkady et al. (2020) Harris Hawks Optimization (HHO) is used to set the PI controller's parameters optimally for DVR, and the outcomes are confirmed in a MATLAB Simulink. Liu et al. (2024) developed a DVR voltage compensation scheme efficiently mitigates for voltage sag, however the focus on voltage sags may restrict its usefulness for other prominent power quality issues. Joshi et al. (2024) compared PI and ANN control method for DVR control, however they do not specify different types of loads and also the only THD is considered as performance matrix. This observation suggests that the system may exhibit reduced robustness in managing a broader spectrum of power quality disturbances. Li et al. (2022) proposed two-stage DVR with a proportional integral resonance controller to improve output power quality under nonlinear load conditions conversely its use for other types of loads, such as linear or mixed loads limits the applicability of the proposed control strategy in broader scenarios. Janardhanan et al. (2022) discusses about SOGI-based PV-DVR system for voltage imbalance mitigation but it does not comprehensively address how fluctuating levels of nonlinear loads might affect the performance of the system under consideration which could be a critical factor in its overall efficacy. Prasad et al. (2024) discussed implementation of stochastic gradient based adaptive control algorithm for improving power quality in Solar PV systems, however they have not addressed how these algorithms perform under sudden load changes or faults in system. Authors in Kumar et al. (2024) presented an ANN and ANFIS algorithm to improve compensatory capabilities of DVR. The study addresses a number of statistical indices, including Mean Square Error (MSE) and Total Harmonic Distortion (THD), but it doesn't offer a thorough evaluation of how these measurements stack up against other approaches already in use. It could be challenging to completely evaluate the benefits and drawbacks of the suggested strategy due to the absence of comparison study. For, over sixty years, researchers and practitioners have studied and implemented SMC because of its versatility. The SMC uses a discontinuous control that is imposed to generate an attractive zone near a fixed switching manifold (also known as a sliding manifold). The switching manifold is used to find the best sliding mode, which is informed by the expected control performance. To impose the ideal sliding motion, the discontinuous control must change indefinitely (Yu and Efe, 2015). Significantly impactful research has meticulously documented the development of SMC theory and its various applications. Several

SMC theories have been developed thus far, with the asymptotic stability-based Lyapunov theory providing the foundation for many of the key concepts, including the linear switching manifolds that characterize expected control performances (Utkin et al., 2020). The concept of asymptotic stability, however, suggests that the slower the state converges to equilibrium, the more distant it is from equilibrium during the dynamical evolution of the system. That means indefinite amounts of time will never result in the system's state being in a state of equilibrium. In practice, this might not be a problem, but it does show that a greater control force is needed if significantly higher steady-state accuracy is desired, which might be unattainable if control action is constrained. In general, acceptance of any degree of non-smoothness in dynamics is used as a criterion for design. Terminal Sliding Mode Control (TSMC) was primarily projected for second-order electronics in the early 1990s, it later evolved to cover a class of Multi Input Multi Output(MIMO) schemes and higher-order Single Input Single Output(SISO) systems (Zhihong and Yu, 1996). The Fast TSMC (FTSMC) system offers many advantages, including high robustness and quick reaction. Its whispering problem, on the other hand, cannot be overlooked, since it might lead to system instability. For practical applications, it's exclusively critical to decrease chattering in the SMC technique. The problem may be solved using a variety of methodologies, including high-order SMC, the boundary-level approach, and the reaching law scheme (Hou et al., 2018). The primary cause of chattering is found to be the state of the system not attaining an equilibrium point. To reduce chattering, the reaching law technique may directly manage the approaching process at the sliding surface (Wang et al., 2019). For chattering reduction, a variety of reaching rules for the SMC was designed to address the concerns mentioned above. Gao and Hung (1993) presented certain reaching laws, for instance, the exponential reaching law, the power reaching law, and the constant reaching law. The classical SMC has certain promising features, including a fast dynamic response, and high robustness to parameter fluctuations, which make it a serious candidate.

The literature studied so far shows that the dynamic nonlinear load conditions are not considered and not all performance metrics are explored. The primary goal of this paper (work) is to demonstrate operation of DVR for dynamic and mixed load scenarios using diverse control algorithms and carrying out comparative result analysis with various performance indices. The linear control algorithm employed is PI with parameter determined from optimization techniques like Particle Swarm Optimization (PSO), Genetic Algorithm (GA) and Mind Blast Algorithm (MBA). Further controller is designed with the non-linear control algorithm SMC which are then extended to TSMC.

A novel concept called Fast Terminal Sliding Mode Control (FTSMC) is introduced and proposed. This new controller ensures improvement in dynamic response, reduced control circuit complexity and improvement of steady-state inaccuracy in the load voltage. In traditional SMC, the power of reaching law has the potential to minimize chattering, but its implementation is gradual. In this paper, to the power reaching law, a linear term is added to speed up convergence away from the sliding surface. It is possible that the power reaching law's efficiency can be improved and the chattering amplitude can be reduced by linearly combining two power terms to create a double power reaching law, whose outcome is speeding up the rate of convergence hence the name fast TSMC. Furthermore, Artificial Neural Network (ANN) method is considered for comparative analysis of findings of research.

This paper structure is shown in **Figure 1** and is organized as follows: In Section 1, the literature survey is elaborated and proposed approach is briefed. In the Section 2, the DVR is explained focusing on the working principle and operation. Also, it details about the controller design based on SMC combined with Synchronous Reference Frame Theory (SRFT). A mathematical average model of the DVR is derived and the reference signal is generation method is explained. By referring average model, sliding mode controller is designed to obtain a non-linear control law. Furthermore, the concept of TSMC is introduced and extended to proposed method, FTSMC. The Section 3 emphasizes different optimization techniques like

PSO, GA and MBA used for PI parameter estimation. The simulation case study is discussed in Section 4 for different load conditions and types of voltage sags by employing different control strategies like PI-PSO, PI-GA, PI-MBA, SMC, TSMC, FTSMC and FTSMC-ANN, results are presented. To evaluate robustness of the proposed system Harmonic Compensation Ratio (HCR) is computed and compared. The quantitative analysis is done by calculating the Sag Score (SS) and Voltage Sag Lost Energy Index (VSLEI). The results and discussions are presented in Section 5. Finally, conclusion is provided in Section 6.

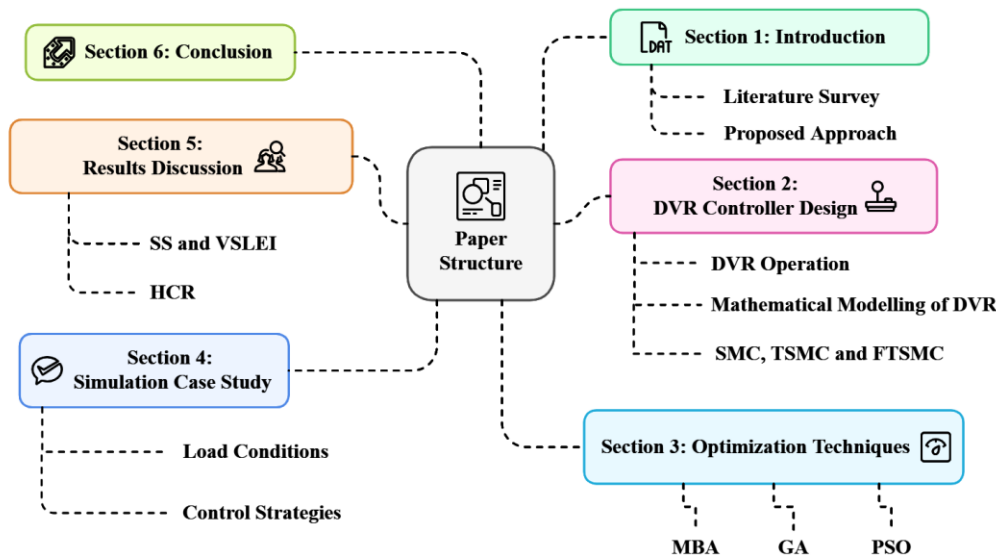


Figure 1. Structure of paper.

2. DVR Controller Design Based on Sliding Mode Control Combined with SRF Theory

2.1 The Concept and Operation of Dynamic Voltage Restorer

When the voltage at the source is uneven or distorted, a DVR can inject a voltage of the proper magnitude and frequency to restore the voltage at the load to the correct amplitude and waveform. Under the supervision of an external regulator, the load side active and reactive power can be generated or absorbed independently at load side of DVR. A solid-state DC-to-AC switching power converter injects three-phase AC output voltages which are in phase with voltages. The DVR is at idle state when there is no fault, however, the normal operating voltage of the system will be measured against the fluctuations that may occur during an outage which will aid to decide the necessary differential voltage injection to retain the load voltage within acceptable ranges. The injected voltages from the dynamic voltage restoration can have their amplitude and phase angles about the distribution grids changed to control the reactive and real power flow. A DVR receives power from a suitably sized energy storage device, connected to its DC input terminal. Under situations where AC passive reactive components are required, the DVR is able to exchange the reactive power required to the distribution system. The DC input terminal of the DVR must be linked to such a source or system to permit the real power transfer between the AC output terminal and distribution system. The application of DVR used in two feeder system is shown in the **Figure 2**. This system is emulated in simulation environment in Section 4 to study the operation of DVR under various load conditions.

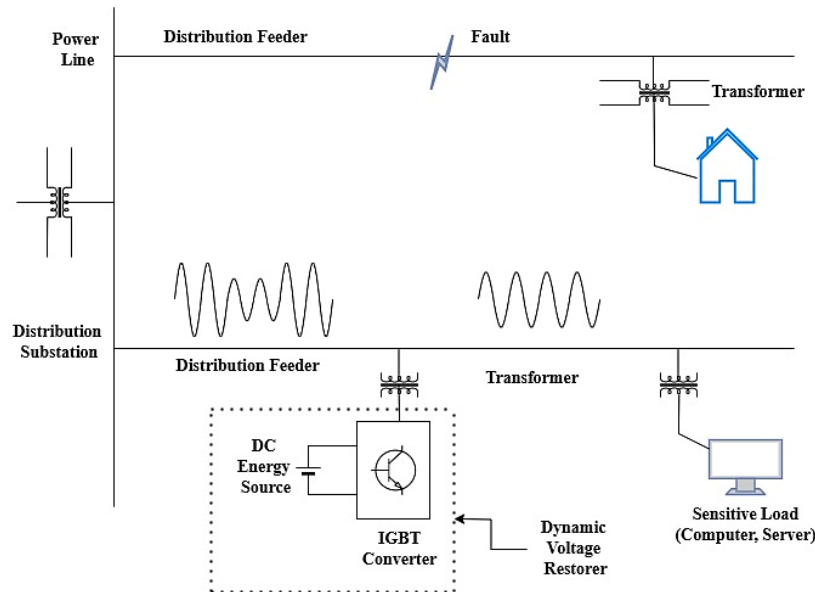


Figure 2. Concept diagram of dynamic voltage restorer.

The block diagram DVR system is elaborated **Figure 3** which consists of the power circuit and control circuit. The power circuit consists of an AC voltage source (V_s), a load (Z_L) and a CT. In contrast, the control circuit consists of a DC voltage source, the VSI, PLL, a RVG, an IC. The similar approach is used to develop the control model for DVR in simulation environment.

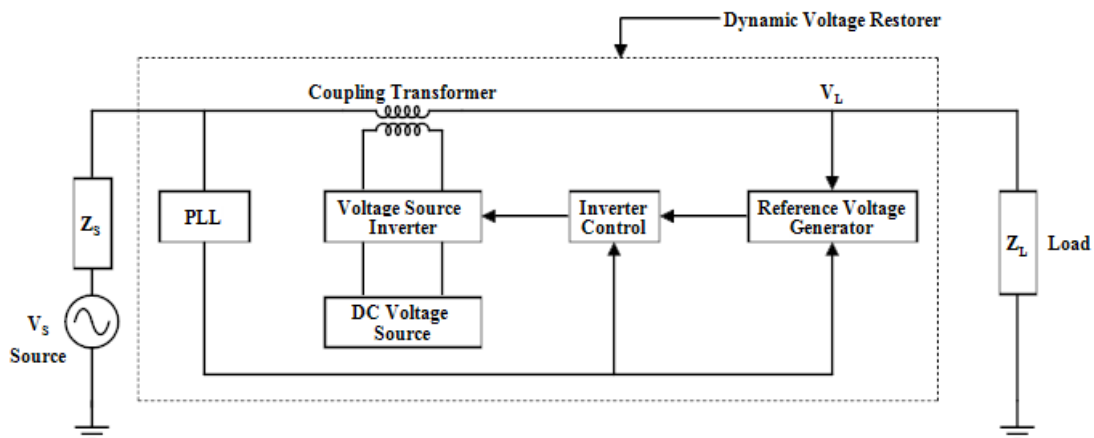


Figure 3. Block diagram of DVR.

An integral component of every DVR is the inverter control. Precise firing pulses are essential for the operation of power electronic switches utilized in the inverter design. These pulses necessitate the development of an accurate mathematical model. The subsequent sections will elucidate the details of research conducted on a mathematical model for the construction of a DVR controller. **Figure 4**, show generalised flow chart to design the DVR control strategy. It is based on Synchronous Reference Frame Theory (SRFT). At first the sinusoidal line voltage, V_{abc} is measured, it is then converted to stationary frame by performing transformation abc to $dq0$ and compared with reference signal. The error signal

extracted is converted back to abc for PWM generation required for VSI to produce missing component of load voltage and added back to load voltage to improve the voltage profile. Here controller is key component, designed by considering different control methods like PI control, SMC, TSMC, FTSMC and ANN.

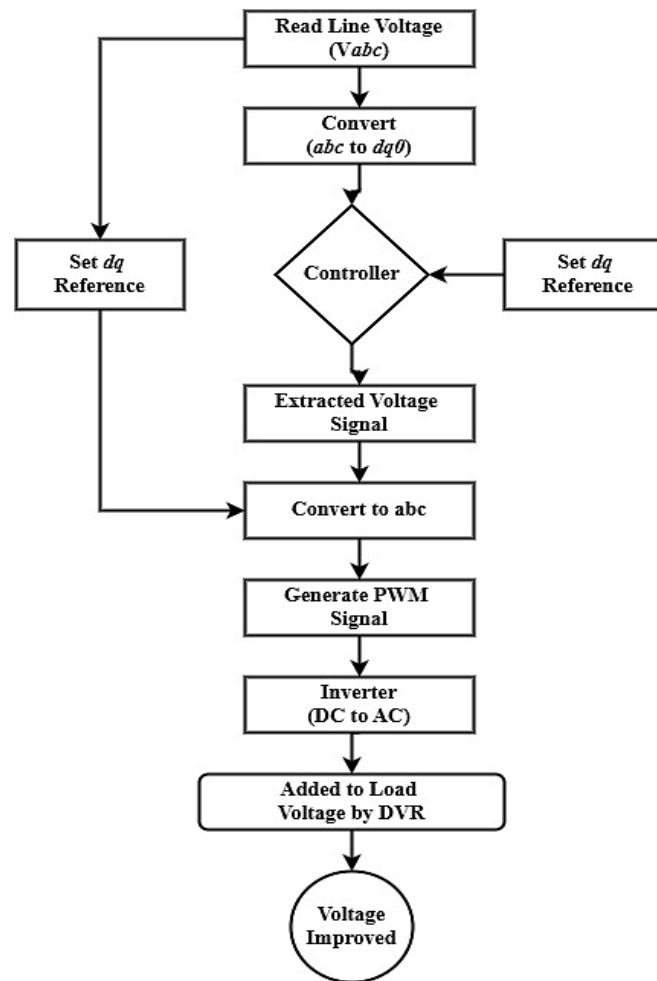


Figure 4. Flow chart of DVR control.

2.2 Average Mathematical Model of DVR

The average mathematical model is derived by referring Rahmani et al. (2006). This is achieved by the series filter generating compensatory voltages V_{comp} for each phase, which are then used to cancel out the load voltage harmonics. The resulting electrical equations are used in the average modelling approach. Several controller-side state variables are used in the model's development. A vector transform matrix is utilized to reduce the system's order to enhance the control design. All state variables are changed to a Synchronously Rotating Frame (SRF) to achieve this ($d, 0, q$). When the inverter legs are averaged with the transformation ratio held constant at 1:1, the whole average model is obtained.

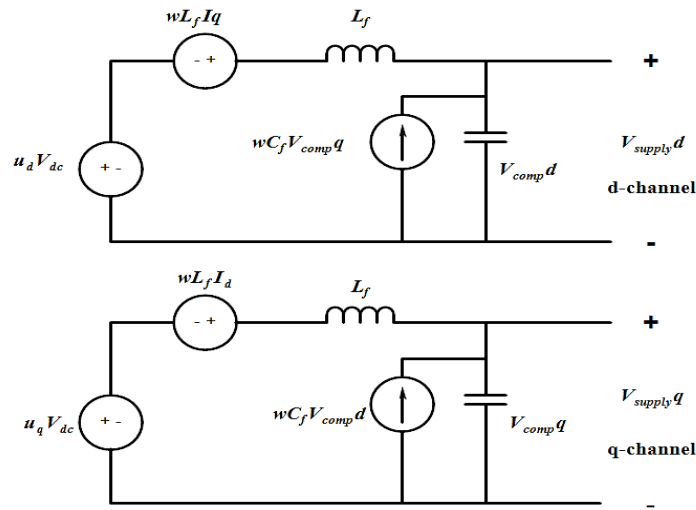


Figure 5. An average model of inverter leg.

When lossless inductors are used, the impact of resistance is ignored. In **Figure 5**, L_f and C_f stands for the filter inductance and capacitance respectively, while I_d and I_q stand for the three-phase source current's d - and q -components respectively. Below are some differential equations that describe the mathematical dynamic model for DVR in such a synchronous reference frame:

$$\frac{di_{compd}}{dt} = \frac{V_{compd}}{L_f} + \omega i_{compq} - \frac{u_d V_{dc}}{L_f} \quad (1)$$

$$\frac{di_{compq}}{dt} = \frac{V_{compq}}{L_f} - \omega i_{compd} - \frac{u_q V_{dc}}{L_f} \quad (2)$$

$$\frac{dV_{compd}}{dt} = \omega V_{compq} - \frac{i_{compd}}{C_f} + \frac{i_{supplyd}}{C_f} \quad (3)$$

$$\frac{dV_{compq}}{dt} = -\omega V_{compd} - \frac{i_{compq}}{C_f} + \frac{i_{supplyq}}{C_f} \quad (4)$$

where, V_{compd} and V_{compq} are the dq -axis compensating voltages, u_d and u_q is the dq -axis duty ratio, and ω is the angular frequency of the source voltage. The following state equation depicts the controller design.

$$\left. \begin{aligned} x &= f(x) + g(x)u \\ y &= h(x) \end{aligned} \right\} \quad (5)$$

The state vector is, $x = [i_{compd}, i_{compq}, V_{compd}, V_{compq}]^T$, the control vector is, $u = [u_d, u_q]^T$, and the output vector $y = [y1, y2]^T = [V_{compd}, V_{compq}]^T$. The state model contains the formulas for multiplying the state variables by the control variables, thus it is evident that the MIMO system is nonlinear. Also, the correlation of the state variable is high. These two problems are precisely solved by the design of the sliding-mode controller.

2.3 Acquisition of Reference Voltage Signal

The control strategy used in this research is constructed by sensing source current (Swain and Ray, 2016). An equivalent circuit of a DVR with a non-linear load is as in **Figure 6**.

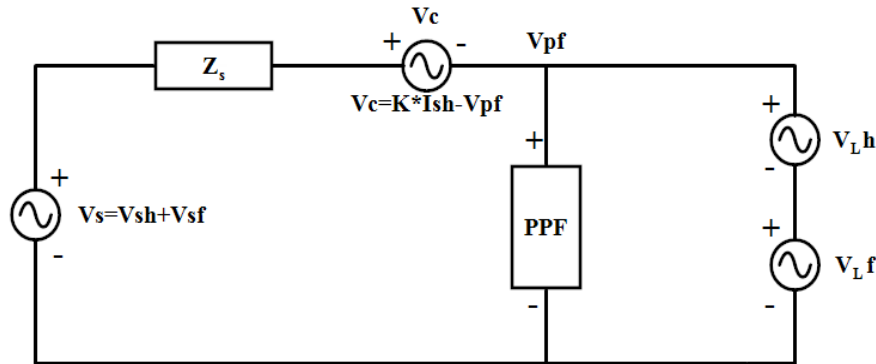


Figure 6. Equivalent circuit of DVR.

The fundamental and harmonic components of the source voltage, V_{sf} & V_{sh} , are presented here. V_{pf} is the voltage across the shunt passive filter. Harmonic & fundamental components of source current are denoted by the symbols I_{sh} & I_{sf} . V_L denotes the voltage of the load. The fundamental and harmonic load voltage components are denoted by V_{Lf} & V_{Lh} , respectively. A controlled voltage source, the DVR generates V_c^* to act as a compensatory voltage.

$$V_c^* = k I_{sh} \quad (6)$$

Applying Ohm's law, the source current harmonic component is as

$$I_{sh} = \frac{V_{sh} - V_{Lh}}{Z_s + k} \quad (7)$$

The variation in I_{sh} is governed by k , control gain. Using the source current detection technique based on the SRF theory, the compensating signal V_c^* is derived as

$$u_d = k I_d \quad (8)$$

$$u_q = k I_q \quad (9)$$

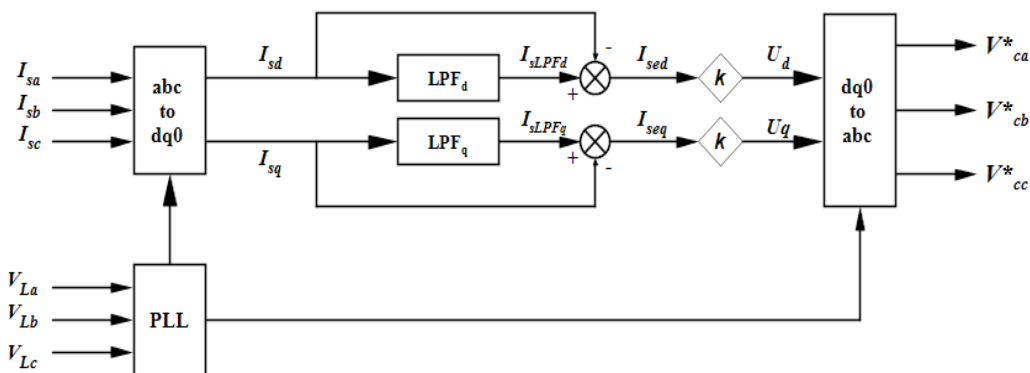


Figure 7. V_c^* schematic representation.

As shown in **Figure 7**, source currents I_{sa} , I_{sb} , I_{sc} are used to derive reference voltages V_{ca}^* , V_{cb}^* , V_{cc}^* respectively. At first stage, sinusoidal source currents are converted to stationary components by park transformation and then passed through low pass filters to have pure DC component, then difference of

unfiltered and filtered signals is multiplied by control gain to derive stationary voltages, finally inverse Park Transformation is used to convert derived voltage from stationary frame to sinusoidal state. For, synchronization of source current with grid voltage phase and frequency the PLL is used.

2.4 Sliding Mode Controller Design with SRF

This average model derived in previous section is then used to generate the sliding mode controller's design. When the control variables u_d and u_q exist independently, the compensating voltages from Equations (3) and (4) are differentiated concerning time, yielding the following equations:

$$\frac{d^2 V_{compd}}{dt} = -\omega^2 V_{compd} - \omega \frac{i_{compq}}{Cf} + \omega \frac{i_{supplyq}}{Cf} - \frac{V_{compd}}{LfCf} - \omega \frac{i_{compq}}{Cf} - \frac{u_d v_{dc}}{LfCf} + \frac{di_{supplyd}}{dt} \cdot \frac{1}{Cf} \quad (10)$$

$$\frac{d^2 V_{compq}}{dt} = -\omega^2 V_{compq} - \omega \frac{i_{compd}}{Cf} + \omega \frac{i_{supplyd}}{Cf} - \frac{V_{compq}}{LfCf} - \omega \frac{i_{compd}}{Cf} - \frac{u_q v_{dc}}{LfCf} + \frac{di_{supplyq}}{dt} \cdot \frac{1}{Cf} \quad (11)$$

Equations show that it is clear Equations (10) & (11) thus at a second derivative of compensatory voltage, the control variables u_d & u_q are derived. As a result, the system is of relative degree 2. Equation's linearized model is used to construct the sliding-mode controller. The series controller is used to induce the compensatory voltages V_{compd} and V_{compq} , which is the controller's intended control goal. Mathematical descriptions of a sliding surface are as follows:

$$\bar{S} = S + \gamma \dot{S} \quad (12)$$

$$\bar{S}_d = S_d + \gamma \dot{S}_d \quad (13)$$

$$\bar{S}_q = S_q + \gamma \dot{S}_q \quad (14)$$

Here γ indicates positive parameter.

The sliding mode controller is developed using below mathematical expressions.

$$\dot{\bar{S}} = 0 \quad (15)$$

$$\dot{\bar{S}}_d = 0 \quad (16)$$

$$\dot{\bar{S}}_q = 0 \quad (17)$$

The definition of the sliding surfaces is

$$S_d = V_{compd} - V_{compd}^* \quad (18)$$

$$S_q = V_{compq} - V_{compq}^* \quad (19)$$

Using the Equations (16), (17), (18), (19) and replacing values with those from output Equations (3) and (4) the d - q domain control law is achieved as

$$\begin{aligned} u_{dequivalent} = & -(\dot{V}_{compd}^* + \ddot{V}_{compd}^*) + \frac{L_f}{V_{dc}} (cf\omega V_{compd} - i_{compd} + i_{supplyd}) \\ & + \frac{\gamma L_f}{V_{dc}} (-cf\omega^2 V_{compd} - \omega i_{compq} + \omega i_{supplyq} - \frac{v_{compd}}{L_f} - \omega i_{compq} + i_{supplyd}) \end{aligned} \quad (20)$$

$$u_{q_{equivalent}} = -(\dot{V}_{comp}q^* + \dot{V}_{comp}q^*) + \frac{L_f}{V_{dc}}(cf\omega V_{comp}q - i_{comp}q + i_{supply}q) + \frac{\gamma L_f}{V_{dc}}(-cf\omega^2 V_{comp}q - \omega i_{comp}d + \omega i_{supply}d - \frac{v_{comp}q}{L_f} - \omega i_{comp}d + i_{supply}q) \quad (21)$$

The non-linear control law is obtained using the following equations

$$U = u_{q_{equivalent}} + u_{switching} \quad (22)$$

$$U_d = u_{d_{equivalent}} + u_{switching} \quad (23)$$

$$U_q = u_{q_{equivalent}} + u_{switching} \quad (24)$$

By substituting Equation (20) into (23) and Equation (21) into (24), the non-linear control law is obtained and schematic is displayed in the **Figure 8**.

$$u_d = -(\dot{V}_{comp}d^* + \dot{V}_{comp}d^*) + \frac{L_f}{V_{dc}}(cf\omega V_{comp}d - i_{comp}d + i_{supply}d) + \frac{\gamma L_f}{V_{dc}}(-cf\omega^2 V_{comp}d - \omega i_{comp}q + \omega i_{supply}q - \frac{v_{comp}d}{L_f} - \omega i_{comp}q + i_{supply}d) - \varepsilon_{11}sign(S_d) - \varepsilon_{12}sign(\dot{S}_d) \quad (25)$$

$$u_q = -(\dot{V}_{comp}q^* + \dot{V}_{comp}q^*) + \frac{L_f}{V_{dc}}(cf\omega V_{comp}q - i_{comp}q + i_{supply}q) + \frac{\gamma L_f}{V_{dc}}(-cf\omega^2 V_{comp}q - \omega i_{comp}d + \omega i_{supply}d - \frac{v_{comp}q}{L_f} - \omega i_{comp}d + i_{supply}q) - \varepsilon_{21}sign(S_q) - \varepsilon_{22}sign(\dot{S}_q) \quad (26)$$

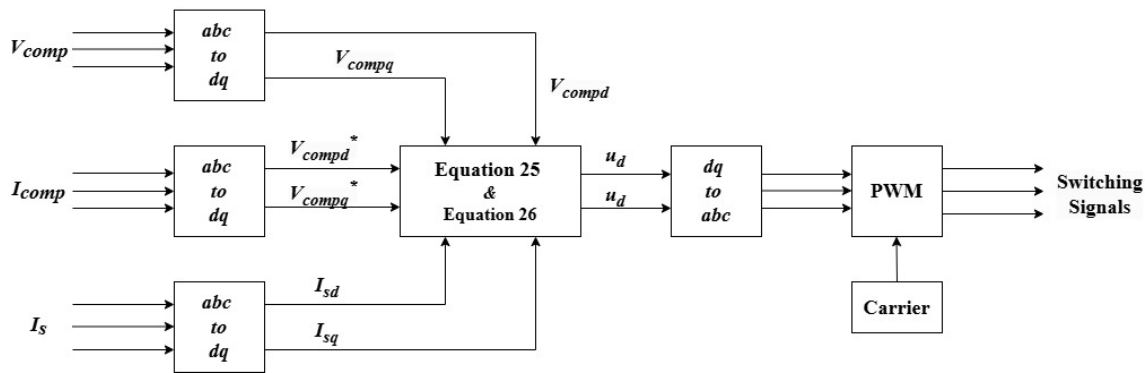


Figure 8. The schematic of a control strategy based on SMC.

The control function of this controller is as follows:

$$U_{eq} = \begin{cases} +1, & \text{when } S > 0 \\ -1 & \text{when } S < 0 \end{cases} \quad (27)$$

2.5 Fast Terminal Sliding Mode Control of DVR

2.5.1 Traditional Terminal Sliding Mode Control

Consider nonlinear sliding surface S

$$S = \dot{x}_1 + \gamma x_1^{p_1/q_1} \quad (28)$$

Here, $\gamma > 0$, $p1$, $q1$ are positive odd numbers such that $q1 > p1$. When the sliding mode equilibrium is reached ($S = 0$) within the finite time t_r , the system dynamics are described as

$$0 = \dot{x}_1 + \gamma x_1^{p1/q1} \quad \text{i.e.} \\ \dot{x}_1 = -\gamma x_1^{p1/q1} \quad (29)$$

It should be noted that the system enters typical sliding mode with $\dot{x}_1 = -\gamma x_1^1$ when $q1 = p1$. The solution of such an equation is $x_1(t) = x_1(t_r)e^{-i\gamma}$ meaning that x_1 approaches the point of equilibrium point ($x_1 = 0$) with exponential rate γ with large value of t ($t \rightarrow \infty$). Once $q1 > p1$, the definite time required to reach equilibrium from $x_1(t_r) \neq 0$ is given by

$$t_s^{TSMC} = \frac{q1}{\gamma(q1-p1)} |x_1(t_r)|^{1-p1/q1} \quad (30)$$

According to Equation (30), x_1 will eventually converge to zero. By "terminal," we mean an equilibrium that can be attained in a finite amount of time. It is also seen that the state of the system involving a non-linear term tends to approach the stability point more rapidly than the state involving a linear term. If the system state is far away from the stability point, it indicates a slow convergence rate.

2.5.2 Proposed Approach: Fast Terminal Sliding Mode Control

In this section new approach is presented to overcome the disadvantages of existing methodologies. The PI based approach has drawback of correct estimation of gain parameters. On the other hand, conventional SMC has drawback of slow convergence rate. To overcome these drawbacks the concept of Fast terminal sliding mode control is presented by Yu and Zhihong (2002), but authors had not applied this mechanism to any general problems. This identified scope is considered and applied for the design of controller for DVR with FTSMC as a novel application. Here, a linear term is introduced to Equation (28) to alleviate the sluggish convergence problem in the TSMC,

$$S = \dot{x}_1 + \alpha x_1 + \gamma x_1^{p1/q1}, \quad \text{where } \alpha > 0 \quad (31)$$

For the proposed method the controller represents mathematical equation obtained when the sliding surface from Equation (31) used to develop control law.

As the system state reaches very extreme away from the stable point, $\dot{x}_1 = -\alpha x_1$ which confirms a high convergence rate. At $S = 0$, the dynamics reduce to $\alpha x_1 = -\gamma x_1^{p1/q1}$ which also shows high convergence. The precise time to attain the equilibrium is calculated by Equation (32)

$$t_s^{FTSMC} = \frac{q1}{\alpha(q1-p1)} \ln \left(\frac{|\alpha x_1(t_r)|^{(q1-p1)/q1 + \gamma}}{\gamma} \right) \quad (32)$$

The proposed approach is explained with the help of **Figure 9**. To derive the non-linear control law with proposed approach the sliding surface equation mentioned in Equation (31) is to be used instead of Equations (13) and (14) to determine equivalent control signals in d -axis and q -axis respectively. Referring to block diagram shown in **Figure 8**, the methodology is explained with following steps:

- Step 1: Acquire reference voltage signals by referring section 2.3.
- Step 2: Determine compensating voltage signals from average model explained in section 2.2.
- Step 3: Use equations of control signals to determine equivalent d -axis and q -axis voltage signals.
- Step 4: Carry out $dq0$ to abc transformation to determine equivalent voltages in time domain.
- Step 5: Compare time domain signals with carrier to obtain pulses for voltage source inverter used in DVR.

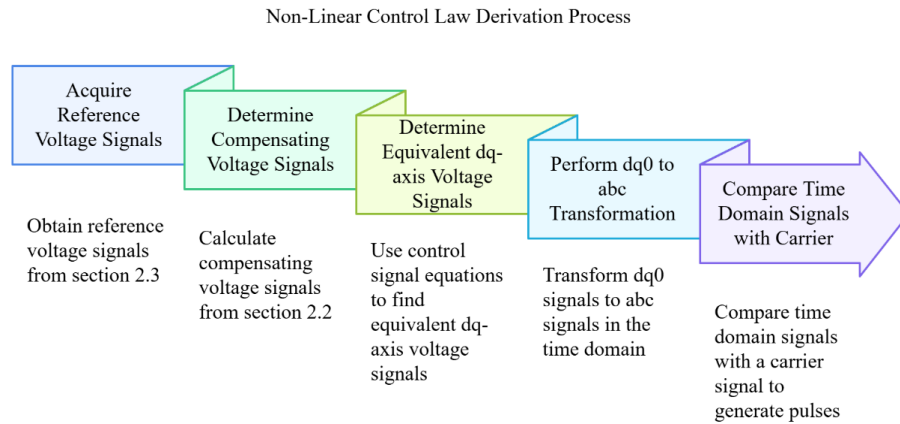


Figure 9. Non-linear control law derivation process.

The proposed approach has several advantages over other methods which demonstrates novelty.

- a) Adaptive: This algorithm is suitable for power quality improvement when the power system is suddenly subjected to disturbances this is because the algorithm can easily adapt system model parameter variations.
- b) Fast Response: This approach has faster convergence rate as compared to other SMC techniques which leads to quicker responses times in power quality issues.
- c) Finite Time Response: Also, it ensures that the system state reaches the equilibrium point in a finite period, as demonstrated by Equation (32).
- d) Complex system performance: Due to complex nature of the power system, the system equation obtained is non-linear in nature. To achieve desired performance of large complex systems the proposed approach is appropriate.

3. Overview of Optimization Algorithms: PSO, GA, MBA for PI Tuning

In this section PI control, which is the most common methodology used for control algorithm design is presented as a baseline for further development of new control approaches. It is well known that PI is a kind of linear algorithm as its transfer function includes proportional, integral and derivative terms which in turn linear in nature (Ang et al., 2005). Most of the times determination of gain values of PI is crucial and time-consuming task. Hence proper optimization technique is to be identified and used. This study examines optimization methods such as PSO, GA, and MBA, owing to their benefits of straightforward implementation and reduced computational burden.

3.1 Particle Swarm Optimization

In the PSO, there exists a group of potential solutions. In multimodal space, every particle has a position vector. A design factor is associated with every dimension. In the multimodal hunt environment, a starting population is produced randomly. Every single particulate is provided with a rate of motion that is produced arbitrarily. The objective function is used to assess every participant's competence. Each particle's location has been determined using the velocity formula, and locations are automatically adjusted. The population's highest fitness function score is noted. Every particle's speed is recalculated. The method terminates when the highest possible fitness number meets the threshold of the convergence condition or when the optimum number of iterations is achieved. The computations representation of this algorithm is illustrated in Equation (33).

$$v_i^{t+1} = wv_i^t + c_1k_1(x_i^{pb} - x_i) + c_2k_2(x_i^{gb} - x_i) \quad (33)$$

where, v_i^{t+1} is the particle velocity for i^{th} iteration, w is weighing function, c_1 and c_2 are weighing factors, k_1 and k_2 are random numbers between 0 and 1, x_i is current position, x_i^{pb} and x_i^{gb} is local best and global best position respectively. Authors (Hassanein et al., 2020) used similar method to determine PI gains used for DVR.

3.2 Genetic Algorithm (GA)

In this type, there is a distinct population size, with respective individuals possessing a unique set of genes. Every collection of genomes represents a proposed solution vector. The vector has an identical quantity of components corresponding to the problem's design variables. At first, a randomly selected population is constructed with design parameters that adhere to the Upper Bound and Lower bound (LB). An objective function is used to assess every member's fitness. Depending upon their fitness, dual-parent followers are chosen after the population. A novel kid is created by either crossing across parental genomes or using the mutational possibility approach to acquire a new chromosomal set which now has faith in the new population to use in the subsequent cycle. This technique is repeated till the convergence conditions are met or the highest possible number of iterations is achieved. The steps are elaborated below (Kassarwani et al., 2018):

- Select the number of control variables (Nc), mutation probability (Mp), maximum number of iterations (i_{max}), population size (Sp) and crossover probability (Cp).
- Fix lower and upper bound for PI controller gains, Kp and Ki .
- Generate random initial population for p individuals.
- Set iteration number $j=1$.
- For every j ranging from 1 to p , decide the values for Kp and Ki .
- Estimate the population's fitness rating and reserve most fit individuals as chromosomes.
- Compute the cumulative, relative and average fitnesses.
- Check out the tournament options.
- On the population, implement both the crossover and mutation operator.
- Change iteration number j and repeat step 5. Save largest fitness as current chromosome. The current chromosome replaces the previous one if its fitness index is greater than the previous one. The replacement number is either fixed or variable and is limited to a third of the whole population.
- Now, replace the old population with current.
- Proceed to step 5 if $j \leq Nc$; if not, this stage yields the best results.

3.3 Mine Blast Algorithm (MBA)

The mine bombs in this method explode, scattering pieces around the search area. An individual fragment goes a distance that is unknown until striking alongside additional mine explosives, triggering a subsequent detonation. The procedure begins by assuming values for design parameters (NV). The total quantity of shrapnel (Nsh) produced by every detonation corresponds to a customized number. The lowest and highest possible values of each design parameter are stated for the problem definition. The design parameters are the output of the problem with respective minimum and maximum bounds. The following steps are to be used as mathematical model. Lower and Upper Bounds (LB and UB) of the design elements are given in the problem and used to formulate initial as defined by Equation (34).

$$X_0 = LB + rand \times (UB - LB) \quad (34)$$

In this case, rand is an arbitrary value that ranges from 0 to 1 and X_0 is the first estimated value of the design variables. At the n th iteration, the location of mine is determined by:

$$X_n = \{X_m\}.$$

In this instance, m ranges from 1 to NV . The detonation at X_n causes the subsequent detonation at X_{n+1} .

$$X_{n+1} = \Delta X + \left(e^{\sqrt{\frac{m_{n+1}}{d_{n+1}}}} \right) X_n \quad (35)$$

ΔX is location of the shrapnel, m_{n+1} is the slope of the shrapnel generated by the initial detonation and d_{n+1} is the distance navigated by the shrapnel since the first detonation.

$$m_{n+1} = \frac{F_{n+1} - F_n}{x_{n+1} - x_n} \quad (36)$$

$$d_{n+1} = \sqrt{(x_{n+1} - x_n)^2 - (F_{n+1} - F_n)^2} \quad (37)$$

F represents the function of X . The d_0 is computed as the difference between UB and LB . Under the constraints of the design variables ($UB > d_0 > LB$), this allows the method to find the optimal solution and ΔX is determined.

$$\Delta X_{n+1} = dn \times rand \times \cos(kv) \quad (38)$$

While iteration is less than the Exploration Factor (Exp) we have,

$$d_{n+1} = dn \times rand^2 \quad (39)$$

$$\Delta X_{n+1} = dn \times \cos(kv) \quad (40)$$

where, $v = \frac{360}{N_{sh}}$ is the angle corresponding to a particular shrapnel k , where k varies from 1 to N_{sh} .

The mining procedure that leads to the global best possible outcome is represented by Equations (36)-(37).

When the minimums are reached, the rate of convergence is rapid since the distance covered by shrapnel has gradually decreased. A pair minimization parameters, A and k is obtained.

$$d_{n+1} = dn \times e^{-\frac{k}{A}} \quad (41)$$

The application of MBA for PI tuning for power system control is described in Majumdar et al. (2014). The performance of MBA is analyzed in Sadollah et al. (2013). **Figure 10**, shows a generalized block diagram for all PI based control schemes. As shown in the diagram, the sinusoidal source and load currents are converted to stationary components from abc to $dq0$ and the difference of stationary components is supplied to the PI controller for generation of the reference voltage. This reference voltage is converted back to the sinusoidal domain to obtain firing pulses for VSI from PWM generator generates.

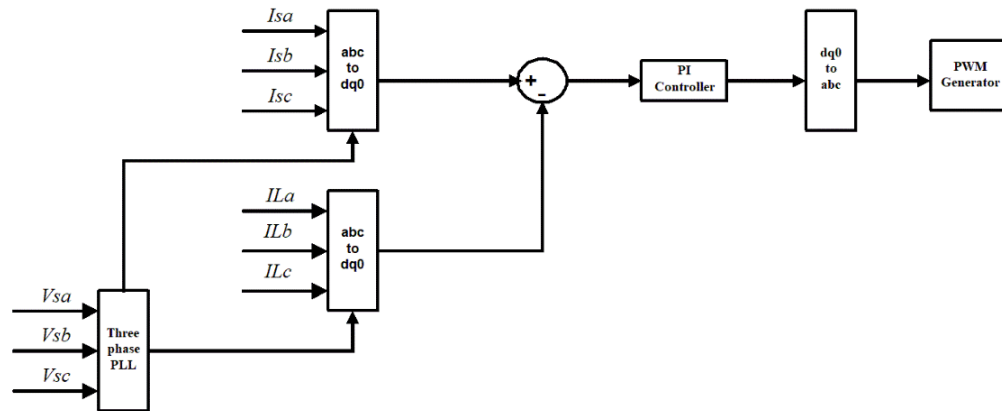


Figure 10. Block diagram of a control strategy based on PI control.

4. Simulation Case Study

The simulation of a DVR with the aforementioned control techniques implemented illustrates the relative investigation by observing the decrease in the amount of Voltage Harmonics and the ability to reinstate the system from Voltage Sag. The simulation parameters are considered from Torres et al. (2019) and provided in **Table 1**.

Table 1. Simulation parameters.

Component	Parameter	Value
Electrical Grid	RMS Source Voltage (line to line)	400 V
	Fundamental Frequency	50 Hz
Coupling Transformer	Apparent Power	20 kVA
	Voltage windings	400 V/400 V
	No load loss	0 (ignored)
Output Filter	Capacitor	8 μ F
	Inductance	6.48 mH
Three Phase Voltage Source Converter	DC link Voltage	600 V
	Carrier Switching Frequency	10 kHz
Load Parameters	Three-Phase Fault Resistance	0.1 Ω
	Linear Load (star connected)	5 kVA, 0.9 pf
	Rectifier load	R= 32 Ω

The line-to-line electrical grid voltage is 400 volts with a fundamental frequency of 50 Hz. The synchronization of DVR with the feeder is done through a coupling transformer of 20kVA by ensuring and keeping the voltage level to 400V with a transformation ratio of 1:1 on both sides of the grid and DVR. The L-C filter is used at the output terminal of the DVR to ensure the frequency of generated voltage is equal to the grid frequency. At the input side of the DVR, the DC voltage is kept at 600 V through a constant voltage source like a battery. The switching frequency used to generate firing pulses is 10 kHz. The values PI controller gains are chosen (Majumdar et al., 2014) for achieving minimum steady-state error, shown **Table 2**.

Table 2. Controller gains.

Algorithm	K_p	K_i
PSO	1.273	0.595
GA	1.272	0.601
MBA	0.998	0.504

Several load cases must be analysed together to conclude. In the world of sags, three-phase imbalanced sags have a special place and are listed in **Table 3** as candidates for simulation study and analysis. Types A, E, and B voltage sags are all taken into account for the comparison.

Table 3. Types of three-phase unbalanced sags.

Case	Fault type	Star connected load	Delta connected load
1	Three Phase	Type A	Type A
2	Two-phase to Ground	Type E	Type F
3	Phase to Phase	Type C	Type D
4	Single Phase	Type B	Type C*

All of the algorithms discussed are considered to analyse the findings. The developed simulation model in MATLAB/Simulink of the system under consideration is illustrated in **Figure 11**. The simulation time is 0.2 seconds. Loads considered are linear three-phase R-L loads and dynamic loads. With a star-connected load, three stages of the LLL-G fault are analysed. Two feeders carrying loads 1 and 2 make up the transmission line. Feeder 1 has a three-phase fault. When there is a failure on feeder 1 between 0.04 and 0.14 seconds (100 ms), the DVR should keep the voltage steady on feeder 2.

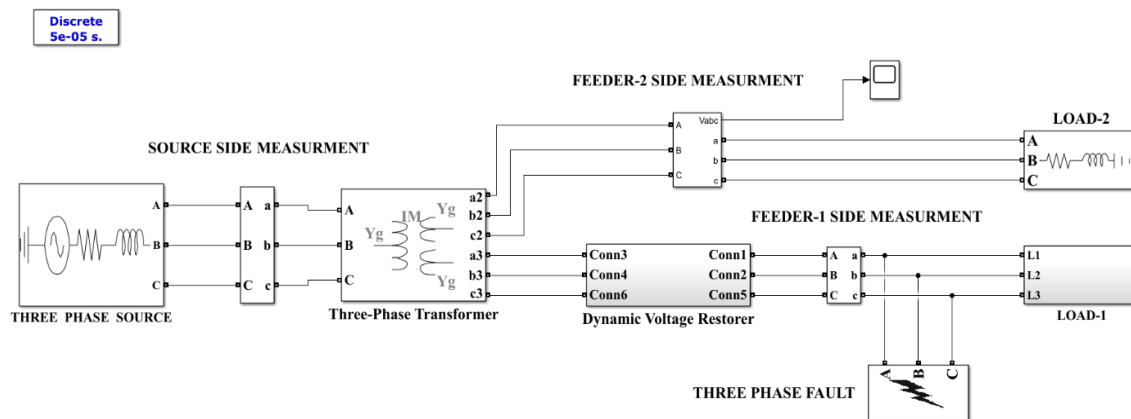


Figure 11. Overall Simulink scheme of DVR.

The uncompensated system is simulated with Type-A Sag with a linear load on feeder-1 having fault resistance of $R_f = 0.1 \Omega$ and the results are obtained. **Figure 12** and **Figure 13** demonstrate the voltage at feeder-1 and feeder-2 individually. **Figure 14** to **Figure 16** shows the voltage THD at feeder -2 for each phase.

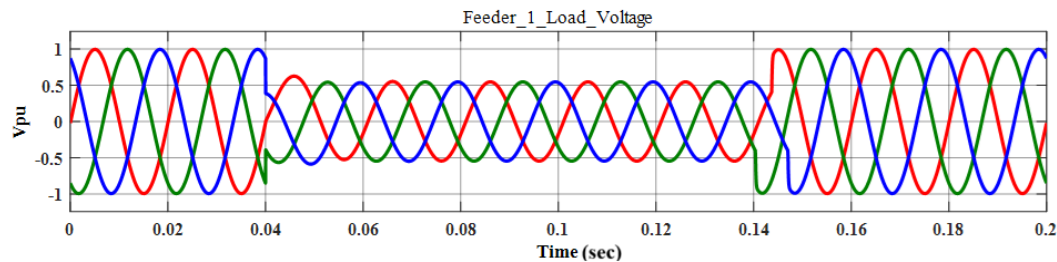


Figure 12. Load voltage of feeder -1 for uncompensated system.

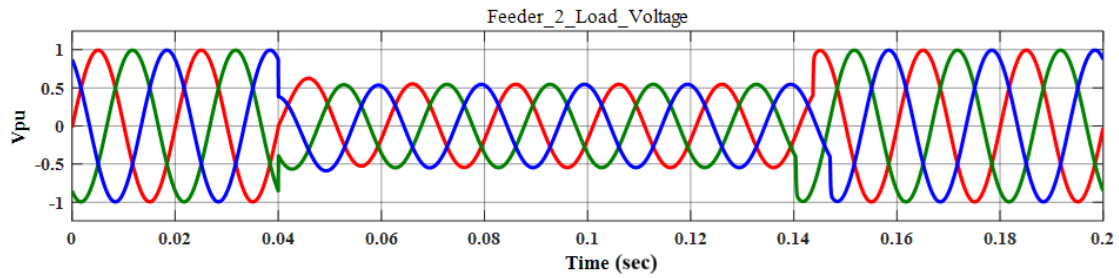


Figure 13. Load voltage of feeder -2 for uncompensated system.

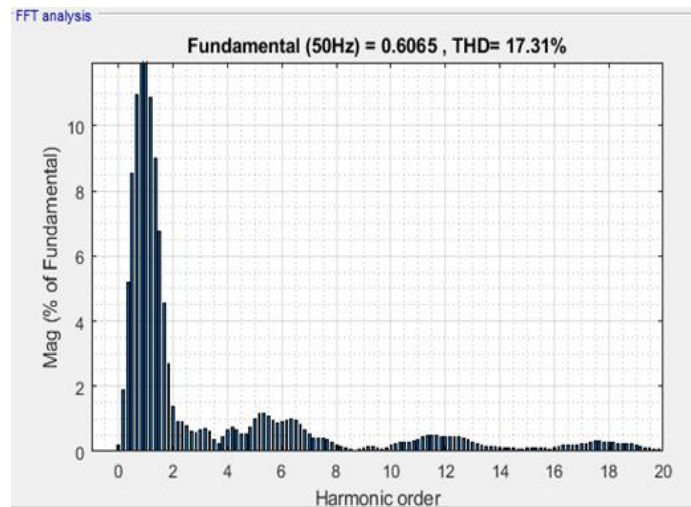


Figure 14. Phase-a load voltage THD of feeder -2 for the uncompensated system.

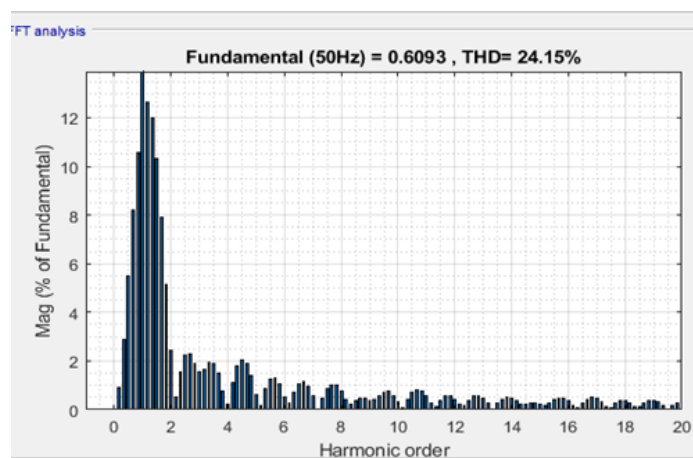


Figure 15. Phase-b load voltage THD of feeder -2 for the uncompensated system.

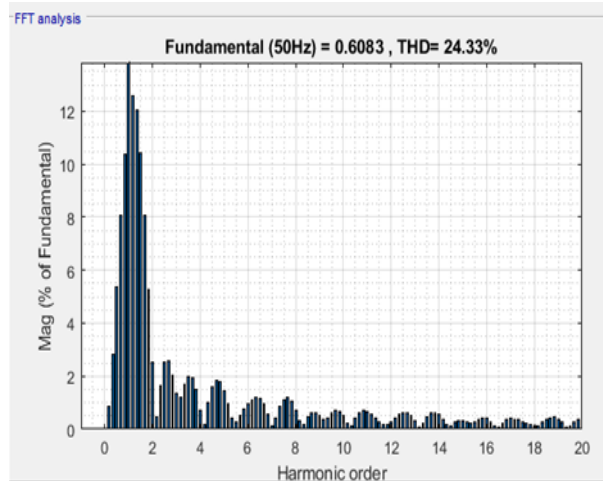


Figure 16. Phase-c load voltage THD of feeder -2 for the uncompensated system.

At first, the compensated systems are simulated by considering a conventional PI-PSO algorithm. **Figure 17** and **18** shows the voltage at feeder-1 and feeder-2 correspondingly, **Figure 19** and **Figure 20** shows the voltage THD at feeder 1 and feeder 2 for phase-a. Though there is a sharp decrease in p.u. the voltage of 0.144 at feeder-1, the controller maintains a voltage of 0.9519 p.u. at feeder-2 which is within acceptable boundaries agreed as per IEEE and THD for phase-a is reduced to 0.83% from 16.14%.

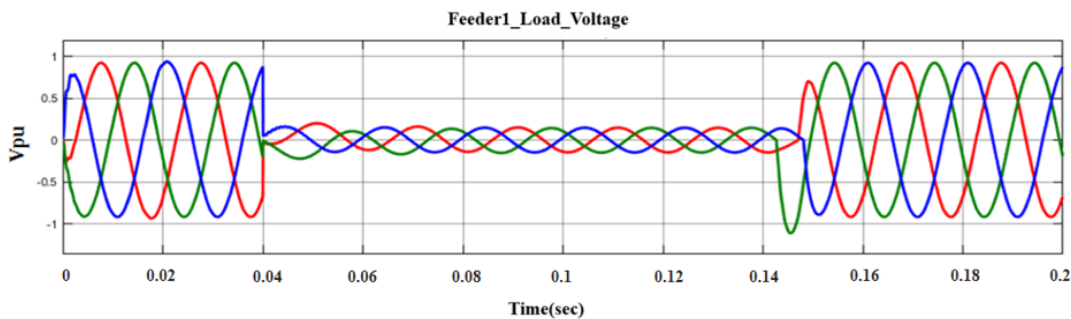


Figure 17. Load voltage of feeder -1 with the PI-PSO algorithm.

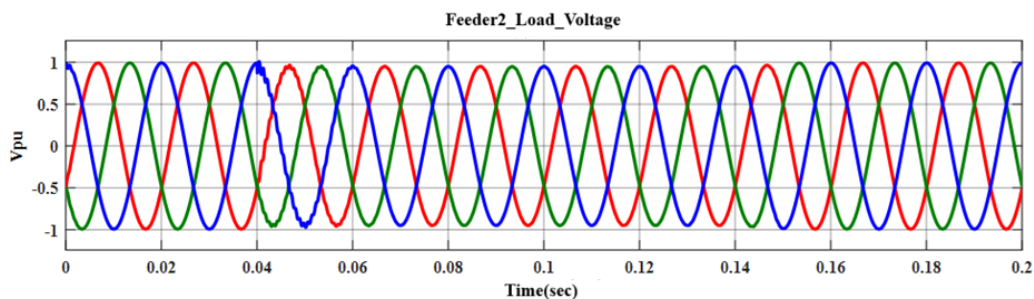


Figure 18. Load voltage of feeder -2 with the PI-PSO algorithm.

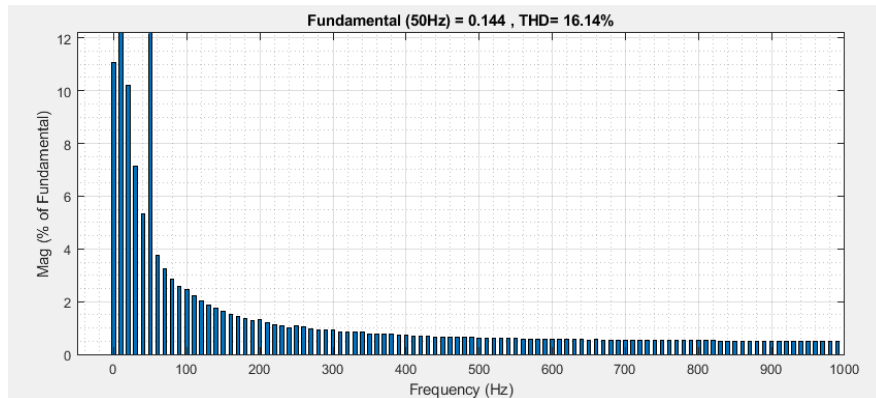


Figure 19. THD of Load voltage of feeder -1 with the PI-PSO algorithm.

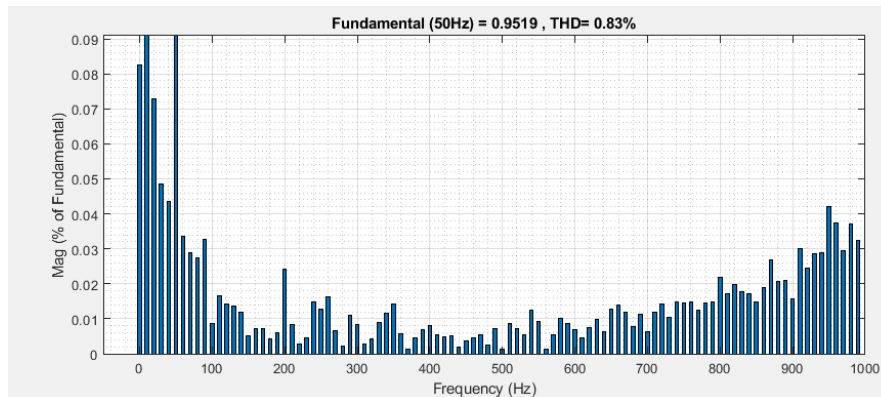


Figure 20. THD of Load voltage of feeder -2 with the PI-PSO algorithm.

The active power flow and reactive power flow is displayed in **Figure 21** and **Figure 22** respectively.

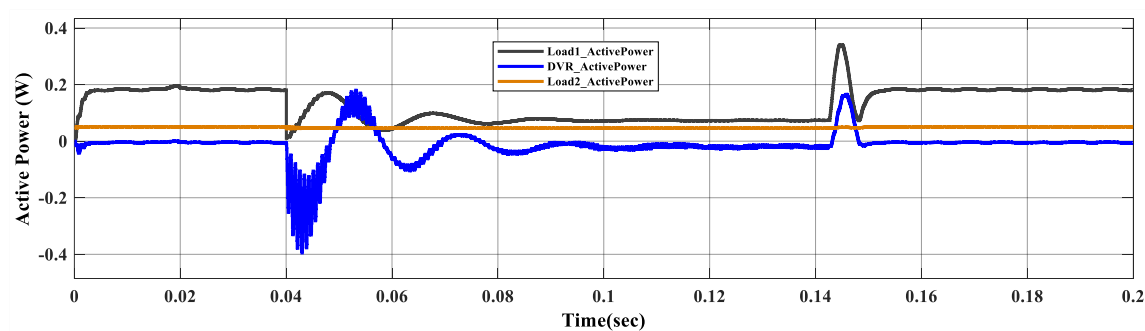


Figure 21. Active power (W) flow during sag period.

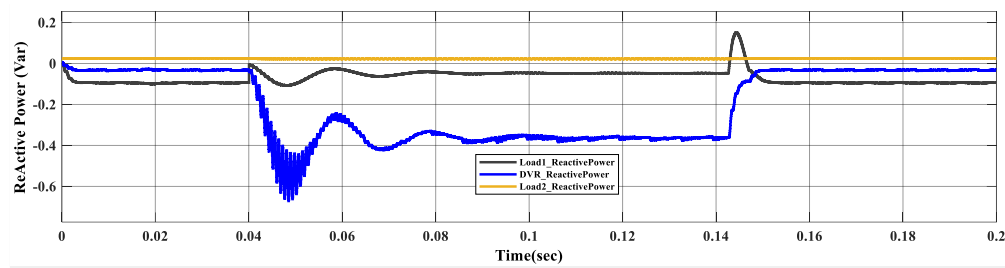


Figure 22. ReActive power (Var) flow during sag period.

Analogous simulations were conducted utilizing the DVR-PI-GA, DVR-PI-MBA and DVR-ANN to record the results. The comparison of proposed strategy with existing the simulation is carried out by considering single feeder system with Type B voltage sag and result is compared against **Figure 22** from (Torres et al., 2019).

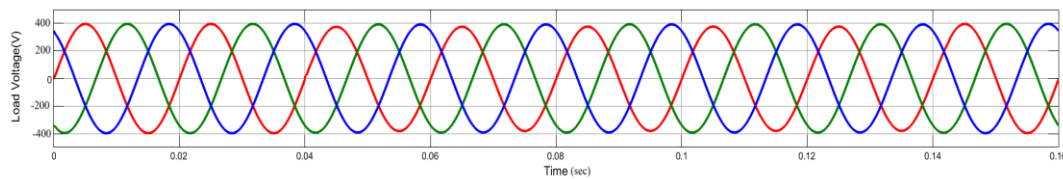


Figure 23. Load voltage with FTSMC-ANN controller.

Figure 23 makes it evident that, the proposed controller performs better than presented in literature. The authors (Torres et al., 2019) have presented only waveform results and not done any comprehensive analysis. Further we observed THD for each phase, the results are promising with phase-a THD as 0.22%, phase-b THD as 0.09 and phase-c THD is 0.11%.

4.1 ANN Based Controller for DVR

The Artificial Neural Network controller used for PQ improvement (Arpitha et al., 2019; Kasala et al., 2021; Sunny et al., 2018) is extended to improve performance of SMC based controller. The multi-layer perceptron (MLP) architecture which is most common is employed to construct the ANN based controller for DVR. This section explains modelling of MLP architecture (Park and Lek, 2016). An input layer, hidden layers and an output layer are among the several levels that make up the MLP. Each layer has a collection of perceptual components called neurons. **Figure 24** illustrates MLP architecture. Every single node exhibits some bias during connections. $X = \{x_1, x_2, \dots, x_n\}$, is the input layer with n variables. The output layer is, $Y = \{y_1, y_2, \dots, y_m\}$ with m variables.

The input from the training data set is sent to input layer which forwards it to the hidden layer. The number of input nodes n in the input layer depends upon the number of dataset features. Every node in hidden layer receives a different input vector variable. The hidden layer is heart of all ANNs. In this layer all calculations of the neural network are included. The node values are multiplied with weights assigned to each hidden layer edge. The activation function is used in this layer. The model may have a couple of hidden layers. Since a small number of hidden layer nodes prevent the model from functioning effectively with complicated input, a number of hidden layer nodes should be correct.

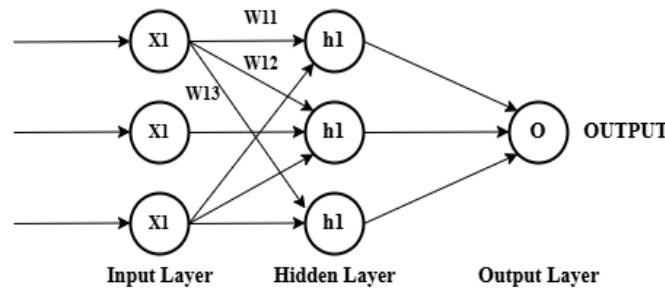


Figure 24. MLP architecture of neural network.

4.4.1 MLP Neural Network Operation

- The attribute of the dataset is represented by input node.
- Every input node sends input attribute value to the hidden layer.
- The input variable is then multiplied with weight associated with every edge in hidden layer and produced results are summed together to create the output.
- The active nodes are identified by using activation function.
- After that the output layer receives the output.
- Next, output layer computes the difference between expected and actual output.
- The model determines expected output by executing back-propagation.

The output MLP can be determined by Equation (42),

$$y = \sum_{j=1}^k \sum_{i=1}^k h_i w_{ij} + \sum_{i=1}^k h_i \quad (42)$$

Here h_k represents hidden nodes in the i th layer.

The objective function (o) used for optimization is given is Equation (43)

$$o_i = g\left(\sum_h w_{h,i} \left(\sum_j w_{j,h} x_j\right)\right) \quad (43)$$

The optimization function $g(x)$ used is sigmoid function illustrated in Equation (44)

$$g(x) = \frac{1}{1+e^{-x}} \quad (44)$$

The Mean Squared Error (MSE) is defined by Equation (45)

$$\text{MSE} = \frac{1}{n} \sum_{i=1}^n (Y_i - \hat{Y}_i)^2 \quad (45)$$

n is number of data points, Y_i and $\hat{Y}_i$ are observed and predicted values respectively.

4.2 Training Results for ANN Based Controller

The nftool in MATLAB is used to create, train and simulate the neural network. The Neural Network type used is similar to shown in **Figure 24** which is two layer feed forward backpropagation with sigmoid hidden function. The network is trained by obtaining training parameters from dataset from conventional PI based simulated model of DVR. The training vectors used to determine d -axis and q -axis compensation signals. The learning rule adopted is Levenberg–Marquardt and performance parameters like Mean-Squared Error, Regression(R) is considered. The training data having regression value close to 1 is chosen and then a Simulink model of trained neural network is generated which then integrated into sliding mode controller.

Table 4. MLP architecture and training parameters.

Architecture	Training parameters
Network Type: Feed Forward Backpropagation The number of layers: 2 The number of neurons on the layers Input: 20, hidden: 20, output: 1 The initial weights and biases: Random Activation functions: Tangent sigmoid	Learning rule: Levenberg-Marquardt Performance: Mean-Squared Error (MSE) Training Function: TRAINLM Adaption learning function: LEARNGDM

4.2.1 *d*-Controller

Initially, the *d*-axis PI controller is replaced with an ANN controller, utilizing the architecture and training parameters outlined in **Table 4**. To achieve optimality, various parameters, including regression and mean square error, are selected. The network is trained until the regression value approaches 1 and the minimum magnitude of MSE is obtained. All training results are summarized in **Table 5**.

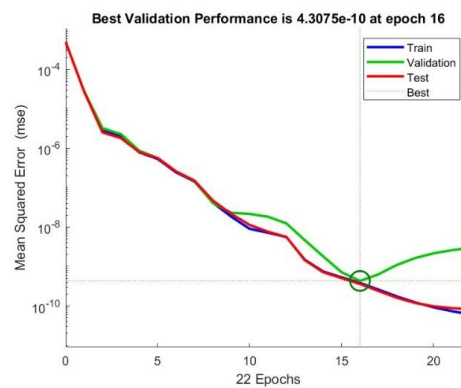
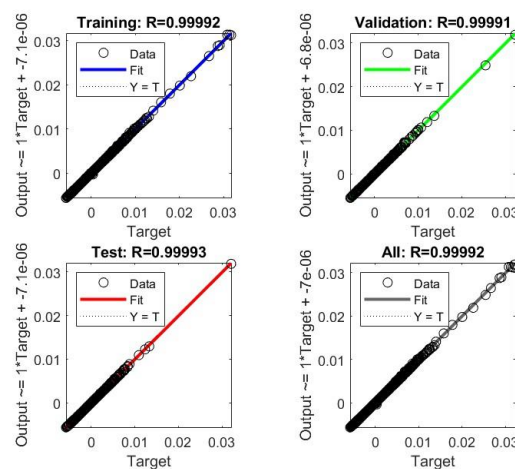
**Figure 25.** Plot of performance (d-axis).**Figure 26.** Plot of regression (d-axis).

Table 5. Training results (d-axis).

Data	Observations	MSE	R
Training	28020	3.8301e-10	0.9999
Validation	6005	4.3075e-10	0.9999
Test	6005	3.6055e-10	0.9999

Figure 25, illustrates the performance plot, which demonstrates the best validation performance at epoch 16 with a validation MSE of 4.3075e-10, **Figure 26**, presents the regression plot obtained with a test R value of 0.99993.

4.2.2 q -Controller

To replace the d -axis PI controller with an ANN controller, the same architecture and training parameters from **Table 4** are applied. To achieve optimal results, regression and MSE are again selected as evaluation metrics. The network is trained until the regression value approaches 1 and the MSE reaches its minimum magnitude. All training results are summarized in **Table 6**.

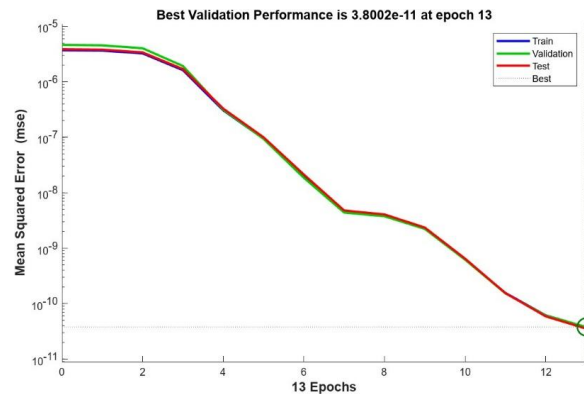
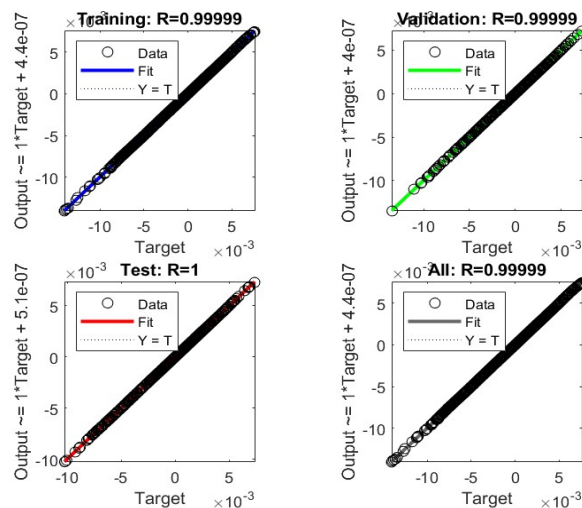
**Figure 27.** Plot of performance (q-axis).**Figure 28.** Plot of regression (q-axis).

Table 6. Training results (q-axis).

Data	Observations	MSE	R
Training	28020	3.7879e-11	1.0000
Validation	6005	3.8002e-11	1.0000
Test	6005	3.5423e-11	1.0000

Figure 27, illustrates the performance plot, which demonstrates the best validation performance at epoch 13 with a validation MSE of 3.8002e-11, **Figure 28**, presents the regression plot obtained with a test R value of 1.

Both d and q trained networks are used to validate the performance of ANN controller. The train R close to 1 indicate that neural network is well trained. The validation of these trained networks is done by replacing PI block in conventional method with ANN block. The validation is said to be successful when controller with ANN has performance equal to or superior than conventional.

5. Result Analysis and Discussions

5.1 Harmonic Indices

5.1.1 Voltage Total Harmonic Distortion (THDV)

The decent quality of output voltage is indicated by waveform harmonic distortion, Equation (46) represents the formula to calculate THDV.

$$THDV = \frac{THDV_a + THDV_b + THDV_c}{3} \quad (46)$$

5.1.2 Harmonic Compensation Ratio (HCR)

The robustness of the proposed system is demonstrated by computing the HCR defined by Equation (47)

$$HCR = \frac{THD \% \text{ after Compensation}}{THD \% \text{ before Compensation}} * 100 \quad (47)$$

5.2 Voltage Sag Indices

The voltage sag indices act as a measure of the restoration of voltage quality. These indices are highly sensitive to any kind of disturbance, so the system's operation is accurately measured. There are various sag indices like the Detroit Edison Sag Score (SS), and Voltage Sag Lost Energy Index (VSLEI).

5.2.1 Detroit Edison Sag Score (SS)

The Sag Score (Bollen, 2000), the first voltage sag index is helpful to have agreement among utilities and consumers, defined by Equation (48)

$$SS = 1 - \frac{V_a + V_b + V_c}{3} \quad (48)$$

where, V_a , V_b , and V_c are per unit rms values of load voltages during the sag period. The recovered voltage after compensation should have a SS value close to 0 (Bollen, 2000). The valid sag has a minimum of one phase with a value equivalent to or slightly less than 0.75p.u.

5.2.2 Voltage Sag Lost Energy Index (VSLEI)

During the sag occurrence period, the load voltage goes below normal, as a result, the energy delivered to the loads is reduced which is computed and indicated by the voltage sag lost energy index defined by Equation (49).

$$VSLEI = \sum_{p=a,b,c} T_p * \left(1 - \frac{V_{ph}}{V_{nom}}\right)^{3.14} \quad (49)$$

where, V_{ph} is a phase voltage, V_{nom} is the nominal voltage for the sag event, and T_p is the sag duration in milliseconds. Various test case scenarios w.r.t. load conditions are taken into account for validation of results obtained when algorithms discussed earlier are implemented in the design of the controller of DVR. The results are illustrated in the following tables case by case.

5.3 Case 1-Linear Load with Power Factor = 0.9

Table 7 represents uncompensated system results. The significant change in load voltage observed ranges from 65 % to 27.08 % for sag types A, E, and B respectively. Also, the voltage THD in each phase is observed, and the mean of all three phases is calculated which is about 17 %. The objective is to minimize the THD and also, to make voltage V_{pu} lesser within acceptable limits. **Table 8** depicts simulated results for minimized THD and HCR. So, it is observed that for type A and B Voltage Sag, FTSMC-ANN algorithm gives better results than others, for type E, all PI and TSMC tied on HCR score.

Table 7. Feeder 1 uncompensated system simulated results.

System	Sag Type	% Dip	Vpu	THDVa	THDVb	THDVc	THDVuncmp
Uncompensated	Type A	65	0.65	11.41	15.58	15.35	14.11
	Type E	51.38	0.51	12.94	15.91	17.83	15.56
	Type B	27.08	0.27	12.33	20.22	17.43	16.66

Table 8. Feeder 2 HCR simulations.

Algorithm	Sag Type	THDVa	THDVb	THDVc	THDVcmp	HCR
PI-PSO	Type A	1.01	0.59	1.53	1.04	0.0739
	Type E	0.51	0.35	0.24	0.37	0.0236
	Type B	0.47	0.25	0.23	0.32	0.0190
PI-GA	Type A	1.01	0.59	1.53	1.04	0.0739
	Type E	0.51	0.35	0.24	0.37	0.0236
	Type B	0.47	0.25	0.23	0.32	0.0190
PI-MBA	Type A	1.01	0.59	1.53	1.04	0.0739
	Type E	0.51	0.35	0.24	0.37	0.0236
	Type B	0.47	0.25	0.23	0.32	0.0190
SMC	Type A	0.81	2.02	2.8	1.88	0.1330
	Type E	0.56	0.66	0.28	0.50	0.0321
	Type B	0.28	0.15	0.17	0.20	0.0120
TSMC	Type A	0.77	1.13	1.72	1.21	0.0855
	Type E	0.33	0.39	0.27	0.33	0.0212
	Type B	0.38	0.22	0.21	0.27	0.0162
FTSMC	Type A	0.3	1.11	1.39	0.93	0.0661
	Type E	0.27	0.59	0.47	0.44	0.0285
	Type B	0.28	0.15	0.18	0.20	0.0122
FTSMC-ANN	Type A	0.29	1.03	1.29	0.87	0.0616
	Type E	0.27	0.57	0.47	0.44	0.0281
	Type B	0.29	0.16	0.19	0.21	0.0128

Figure 29 shows, the plot of HCR. It is clear that for Type B Sag, SMC outperforms other algorithms, for type E Sag, TSMC is better and for type A FTSMC-ANN gives outstanding results.

Table 9, illustrates the results of the SS and VSLEI to check the system performance and **Table 10** comparative analysis, it has been observed that for uncompensated feeder 1, the Sag score varies from

16.63% to 5.76% and VSLEI (J) varies from 1.0832 J to 0.2904 J for sag type A, E, B respectively. While for uncompensated feeder 2, SS varies from 12.00 % to 4.84 % and VSLEI (J) varies from 0.3873 J to 0.0241 J for sag type A, E, and B respectively. With compensation introduced, it has been observed that at the feeder- 2, SS (%) and VSLEI reduced drastically. The SS (%) is reduced by 50% for all sag types. A similar observation is captured for VSLEI, achieving an ideal value close to 0.

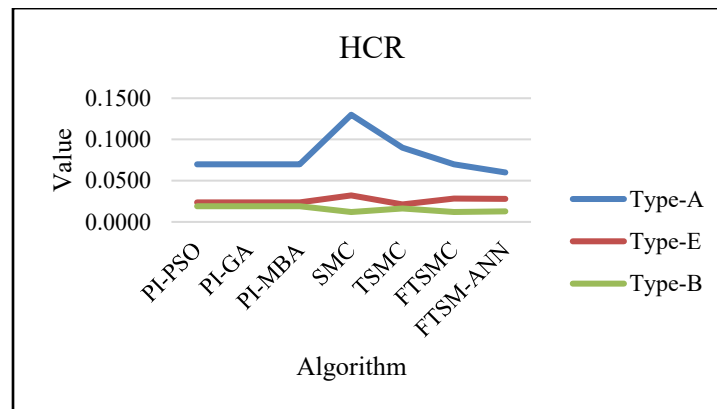


Figure 29. Plot of HCR.

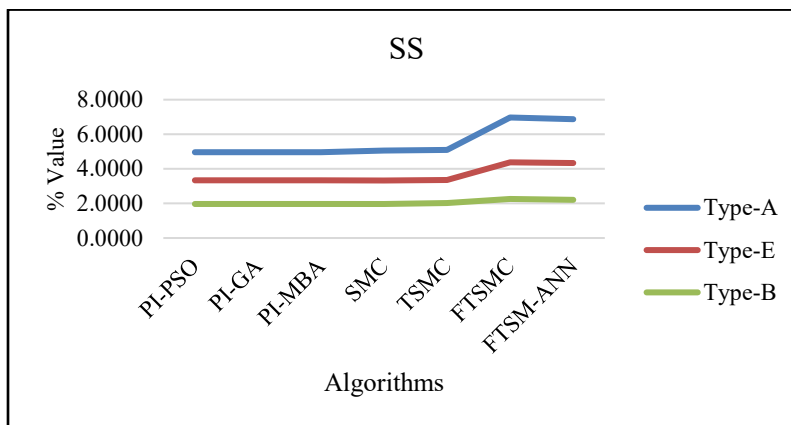
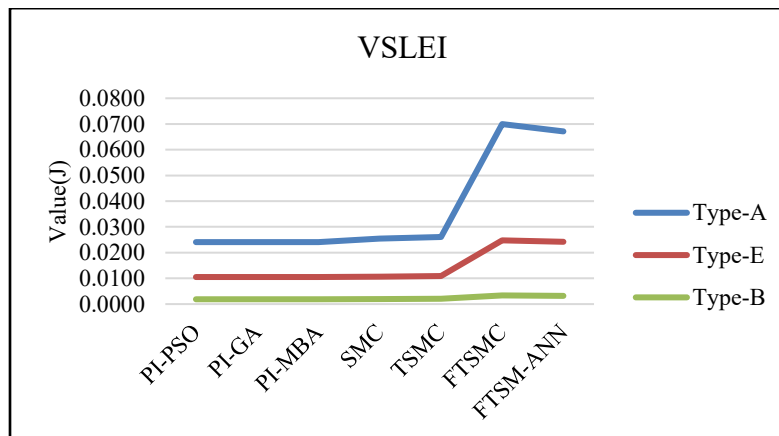
Table 9. Simulation results: SS and VSLEI.

Algorithm	Sag Type	Vpua	Vpub	Vpuc	SS (%)	VSLEI (J)
uncompensated feeder1	Type A	0.8439	0.8338	0.8233	16.63	1.0832
	Type E	0.8447	0.8335	0.9914	11.01	0.6477
	Type B	0.8444	0.9914	0.9914	5.76	0.2904
uncompensated feeder2	Type A	0.8864	0.8785	0.8751	12.00	0.3873
	Type E	0.8668	0.8784	0.994	8.69	0.3121
	Type B	0.8667	0.994	0.994	4.84	0.1787
PI-PSO	Type A	0.9519	0.9520	0.9516	4.96	0.0241
	Type E	0.955	0.9641	0.9841	3.33	0.0105
	Type B	0.9731	0.9829	0.9878	1.97	0.0019
PI-GA	Type A	0.9519	0.9520	0.9516	4.96	0.0241
	Type E	0.955	0.9641	0.9841	3.33	0.0105
	Type B	0.9731	0.9829	0.9878	1.97	0.0019
PI-MBA	Type A	0.9519	0.9520	0.9516	4.96	0.0241
	Type E	0.955	0.9641	0.9841	3.33	0.0105
	Type B	0.9731	0.9829	0.9878	1.97	0.0019
SMC	Type A	0.9495	0.9495	0.9495	5.05	0.0254
	Type E	0.939	0.948	0.981	3.33	0.0106
	Type B	0.971	0.9824	0.9873	1.98	0.0019
TSMC	Type A	0.9492	0.9492	0.9491	5.09	0.0260
	Type E	0.9503	0.9651	0.9832	3.36	0.0109
	Type B	0.9627	0.9658	0.9658	2.02	0.0020
FTSMC	Type A	0.9305	0.9303	0.9301	6.97	0.0700
	Type E	0.9507	0.9652	0.9836	4.38	0.0248
	Type B	0.9646	0.9795	0.9881	2.26	0.0034
FTSMC-ANN	Type A	0.9316	0.9311	0.9309	6.88	0.0672
	Type E	0.949	0.9816	0.9393	4.34	0.0242
	Type B	0.9653	0.9799	0.9884	2.21	0.0032

Table 10. Comparative analysis of all algorithms (linear load).

Algorithm	HCR			SS			VSLEI		
	Type-A	Type-E	Type-B	Type-A	Type-E	Type-B	Type-A	Type-E	Type-B
PI-PSO	0.0700	0.0236	0.0190	4.9633	3.3300	1.9700	0.0241	0.0105	0.0019
PI-GA	0.0700	0.0236	0.0190	4.9633	3.3300	1.9700	0.0241	0.0105	0.0019
PI-MBA	0.0700	0.0236	0.0190	4.9633	3.3300	1.9700	0.0241	0.0105	0.0019
SMC	0.1300	0.0321	0.0120	5.0500	3.3267	1.9767	0.0254	0.0106	0.0019
TSMC	0.0900	0.0212	0.0162	5.0867	3.3633	2.0167	0.0260	0.0109	0.0020
FTSMC	0.0700	0.0285	0.0122	6.9700	4.3767	2.2600	0.0700	0.0248	0.0034
FTSM-ANN	0.0600	0.0281	0.0128	6.8800	4.3367	2.2133	0.0672	0.0242	0.0032

Figure 30 and **Figure 31**, shows the plots of comparative analysis of all methods for Sag score, VSLEI respectively. It is observed that for all types of sags, performance of PI based algorithms is better than SMC based algorithms.

**Figure 30.** Plot of percent sag score.**Figure 31.** Plot of VSLEI.

5.4 Case 2-Dynamic Load with Power Factor = 0.9

In **Table 11**, the voltage THD and HCR results at feeder-2 are demonstrated and shown in **Figure 32**. The observations are that for type-A voltage sag, SMC and TSMC algorithms give better results than others, for type E, PI-PSO proves to be good, and for type B, FTSMC is comparatively best.

Table 11. Feeder 2 HCR simulations.

Algorithm	Sag Type	THDVa	THDVb	THDVc	THDVcmp	HCR
PI-PSO	Type A	1.01	0.59	1.53	1.04	0.0739
	Type E	0.51	0.35	0.24	0.37	0.0236
	Type B	0.47	0.25	0.23	0.32	0.0190
PI-GA	Type A	1.01	0.59	1.53	1.04	0.0739
	Type E	0.51	0.35	0.24	0.37	0.0236
	Type B	0.47	0.25	0.23	0.32	0.0190
PI-MBA	Type A	1.01	0.59	1.53	1.04	0.0739
	Type E	0.51	0.35	0.24	0.37	0.0236
	Type B	0.47	0.25	0.23	0.32	0.0190
SMC	Type A	0.81	2.02	2.80	1.88	0.1330
	Type E	0.56	0.66	0.28	0.50	0.0321
	Type B	0.28	0.15	0.17	0.20	0.0120
TSMC	Type A	0.77	1.13	1.72	1.21	0.0855
	Type E	0.33	0.39	0.27	0.33	0.0212
	Type B	0.38	0.22	0.21	0.27	0.0162
FTSMC	Type A	0.30	1.11	1.39	0.93	0.0661
	Type E	0.27	0.59	0.47	0.44	0.0285
	Type B	0.28	0.15	0.18	0.20	0.0122
FTSMC-ANN	Type A	0.29	1.03	1.29	0.87	0.0616
	Type E	0.27	0.57	0.47	0.44	0.0281
	Type B	0.29	0.16	0.19	0.21	0.0128

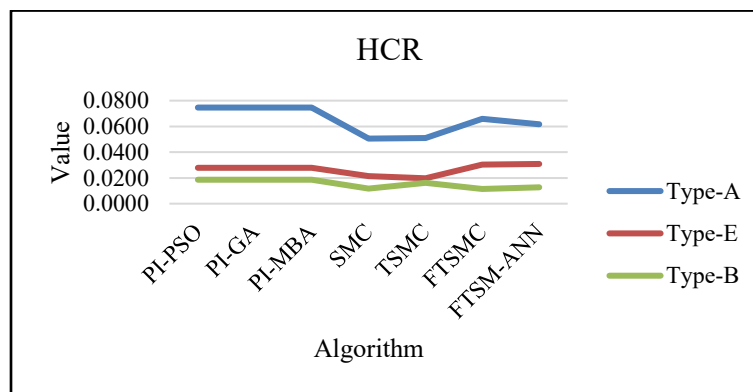


Figure 32. Plot of HCR.

In order to assess the system's performance, **Table 12**, displays the SS and VSLEI data and **Table 13** comparative analysis. It is noted that at feeder-2, both SS (%) and VSLEI significantly decreased. The SS (%) is reduced by 50% for all sag types. A similar observation was found for VSLEI, achieving the ideal value close to 0.

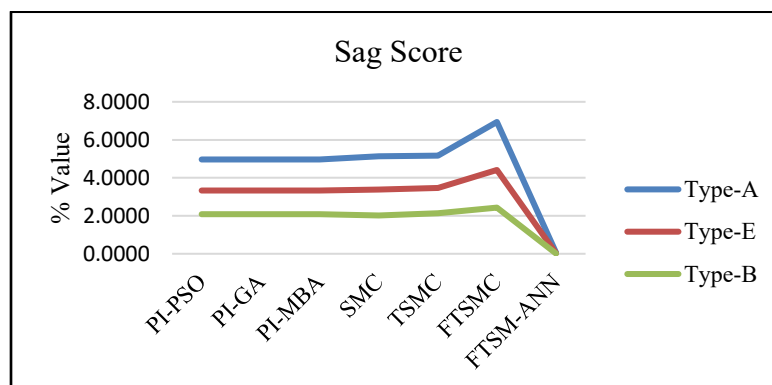
Figures 33 and **Figure 34**, shows the plots of comparative analysis of all methods for Sag score, VSLEI respectively. Considering SS value the FTSMC-ANN performs better than other methods and for VSLEI, PI based methods are good.

Table 12. Simulation results: SS and VSLEI.

Algorithm	Sag type	V _{pua}	V _{pub}	V _{puc}	SS (%)	VSLEI (J)
uncompensated Feeder1	Type A	0.8403	0.83	0.8195	17.01	1.1612
	Type E	0.8162	0.8404	0.9957	11.59	0.8043
	Type B	0.8276	0.9957	0.9957	6.03	0.4006
uncompensated Feeder2	Type A	0.8774	0.8762	0.8753	12.37	0.4239
	Type E	0.8322	0.8525	0.9965	10.63	0.6135
	Type B	0.8456	0.9965	0.9965	5.38	0.2834
PI-PSO	Type A	0.9505	0.9504	0.9503	4.96	0.0240
	Type E	0.9652	0.9838	0.9512	3.33	0.0105
	Type B	0.9706	0.9812	0.9859	2.08	0.0021
PI-GA	Type A	0.9505	0.9504	0.9503	4.96	0.0240
	Type E	0.9652	0.9838	0.9512	3.33	0.0105
	Type B	0.9706	0.9812	0.9859	2.08	0.0021
PI-MBA	Type A	0.9505	0.9504	0.9503	4.96	0.0240
	Type E	0.9652	0.9838	0.9512	3.33	0.0105
	Type B	0.9706	0.9812	0.9859	2.08	0.0021
SMC	Type A	0.9488	0.9486	0.9487	5.13	0.0267
	Type E	0.9507	0.9642	0.9835	3.39	0.0110
	Type B	0.971	0.9824	0.9863	2.01	0.0019
TSMC	Type A	0.9484	0.9484	0.9483	5.16	0.0273
	Type E	0.9502	0.9636	0.9824	3.46	0.0115
	Type B	0.9695	0.9809	0.9855	2.14	0.0023
FTSMC	Type A	0.9308	0.9306	0.9304	6.94	0.0690
	Type E	0.9389	0.9484	0.9803	4.41	0.0249
	Type B	0.9634	0.9777	0.986	2.43	0.0039
FTSMC-ANN	Type A	0.9316	0.9311	0.9309	6.88	0.0672
	Type E	0.9394	0.9484	0.9806	4.39	0.0245
	Type B	0.9644	0.9782	0.9867	2.36	0.0036

Table 13. Comparative analysis of all algorithms (Dynamic load).

HCR				SS			VSLEI		
Algorithm	Type-A	Type-E	Type-B	Type-A	Type-E	Type-B	Type-A	Type-E	Type-B
PI-PSO	0.0746	0.0278	0.0186	4.9600	3.3267	2.0767	0.0241	0.0105	0.0019
PI-GA	0.0746	0.0278	0.0186	4.9600	3.3267	2.0767	0.0241	0.0105	0.0019
PI-MBA	0.0746	0.0278	0.0186	4.9600	3.3267	2.0767	0.0241	0.0105	0.0019
SMC	0.0505	0.0214	0.0118	5.1300	3.3867	2.0100	0.0254	0.0106	0.0019
TSMC	0.0510	0.0197	0.0162	5.1633	3.4600	2.1367	0.0260	0.0109	0.0020
FTSMC	0.0659	0.0304	0.0114	6.9400	4.4133	2.4300	0.0700	0.0248	0.0034
FTSM-ANN	0.0616	0.0308	0.0126	6.8800	4.3867	2.3567	0.0672	0.0242	0.0032

**Figure 33.** Plot of percent sag score.

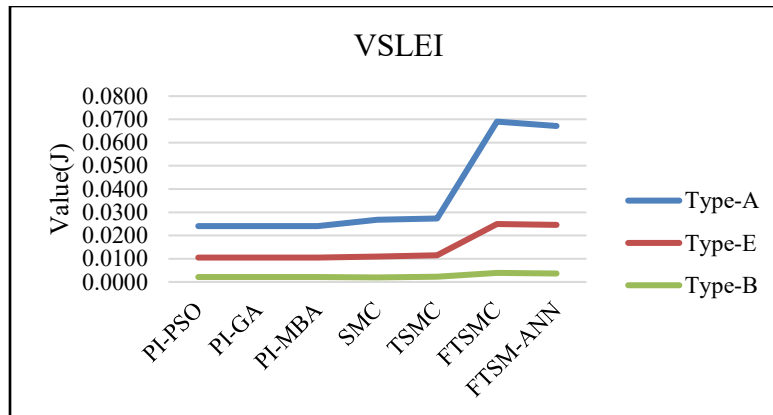


Figure 34. Plot of VSLEI.

5.5 Case 3-Combined Load Conditions

In **Table 14**, the combined load condition is considered; Voltage THD and HCR result at feeder-2 are illustrated and plotted in the **Figure 35**. The observations are that for type-A voltage sag, the FTSMC algorithm gives better results than others, for Type E, PI-MBA, and FTSMC have tied but PI-PSO proves to be superior, and for type B, FTSMC outperforms others.

In **Table 15**, results of the SS and VSLEI to check the system performance are shown and in **Table 16** comparative analysis, it has been observed that for uncompensated feeder 1, the sag score varies from 66.34% to 22.84% and VSLEI (J) varies from 82.7132 J to 29.2709 J for sag type A, E, B respectively. While for uncompensated feeder 2, sag score varies from 45.14 % to 14.74 % and VSLEI (J) varies from 24.6970 to 2.0753 for sag type A, E, and B respectively. With compensation introduced, it has been observed that at the feeder- 2, SS (%) and VSLEI reduced drastically. The SS (%) is reduced by 50% for all sag types. A similar observation was found for VSLEI, achieving value close to 0.

Table 14. Feeder 2 HCR simulations.

Algorithm	Sag Type	THDVa	THDVb	THDVc	THDVcmp	HCR
PI-PSO	Type A	1.01	0.59	1.53	1.04	0.0727
	Type E	0.51	0.35	0.24	0.37	0.0778
	Type B	0.47	0.25	0.23	0.32	0.0842
PI-GA	Type A	1.01	0.59	1.53	1.04	0.0727
	Type E	0.51	0.35	0.24	0.37	0.0778
	Type B	0.47	0.25	0.23	0.32	0.0842
PI-MBA	Type A	1.01	0.59	1.53	1.04	0.0727
	Type E	0.51	0.35	0.24	0.37	0.0778
	Type B	0.47	0.25	0.23	0.32	0.0842
SMC	Type A	0.81	2.02	2.80	1.88	0.0496
	Type E	0.56	0.66	0.28	0.50	0.0705
	Type B	0.28	0.15	0.17	0.20	0.0768
TSMC	Type A	0.77	1.13	1.72	1.21	0.0496
	Type E	0.33	0.39	0.27	0.33	0.0705
	Type B	0.38	0.22	0.21	0.27	0.0758
FTSMC	Type A	0.30	1.11	1.39	0.93	0.0687
	Type E	0.27	0.59	0.47	0.44	0.0426
	Type B	0.28	0.15	0.18	0.20	0.0724
FTSMC-ANN	Type A	0.29	1.03	1.29	0.87	0.0628
	Type E	0.27	0.57	0.47	0.44	0.0388
	Type B	0.29	0.16	0.19	0.21	0.0610

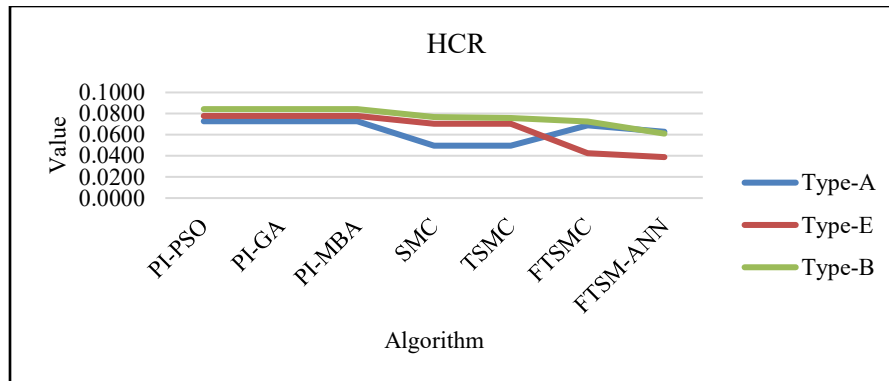


Figure 35. Plot of HCR.

Table 15. Simulation results: SS and VSLEI.

Algorithm	Sag Type	Vpua	Vpub	Vpuc	SS (%)	VSLEI (J)
Uncompensated feeder 1	Type A	0.3403	0.3423	0.3273	66.34	82.7132
	Type E	0.328	0.3404	1	44.39	55.7771
	Type B	0.3238	1	0.9909	22.84	29.2709
Uncompensated feeder 2	Type A	0.5535	0.5477	0.5445	45.14	24.6970
	Type E	0.7363	0.5509	0.8362	29.22	9.9603
	Type B	0.7178	0.8636	0.9764	14.74	2.0753
PI-PSO	Type A	0.9505	0.9504	0.9502	4.96	0.0241
	Type E	0.9469	0.9838	0.9512	3.94	0.0178
	Type B	0.9632	0.9677	0.966	3.44	0.0077
PI-GA	Type A	0.9505	0.9504	0.9503	4.96	0.0240
	Type E	0.9652	0.9838	0.9512	3.33	0.0105
	Type B	0.9706	0.9812	0.9859	2.08	0.0021
PI-MBA	Type A	0.9505	0.9504	0.9503	4.96	0.0240
	Type E	0.9652	0.9838	0.9512	3.33	0.0105
	Type B	0.9706	0.9812	0.9859	2.08	0.0021
SMC	Type A	0.9488	0.9486	0.9486	5.13	0.0268
	Type E	0.946	0.959	0.9637	4.38	0.0179
	Type B	0.9628	0.9672	0.9659	3.47	0.0079
TSMC	Type A	0.9488	0.9486	0.9486	5.13	0.0268
	Type E	0.946	0.959	0.9637	4.38	0.0179
	Type B	0.9628	0.9672	0.9659	3.47	0.0079
FTSMC	Type A	0.931	0.9309	0.9306	6.92	0.0683
	Type E	0.9311	0.9484	0.9803	4.67	0.0320
	Type B	0.9634	0.9777	0.986	2.43	0.0039
FTSMC-ANN	Type A	0.9315	0.931	0.9309	6.89	0.0674
	Type E	0.9394	0.9484	0.9806	4.39	0.0245
	Type B	0.9644	0.9782	0.9867	2.36	0.0036

Table 16. Comparative analysis of all algorithms (combined load).

HCR				SS			VLSEI		
Algorithm	Type-A	Type-E	Type-B	Type-A	Type-E	Type-B	Type-A	Type-E	Type-B
PI-PSO	0.0700	0.0236	0.0190	4.9633	3.3300	1.9700	0.0241	0.0105	0.0019
PI-GA	0.0700	0.0236	0.0190	4.9633	3.3300	1.9700	0.0241	0.0105	0.0019
PI-MBA	0.0700	0.0236	0.0190	4.9633	3.3300	1.9700	0.0241	0.0105	0.0019
SMC	0.1300	0.0321	0.0120	5.0500	3.3267	1.9767	0.0254	0.0106	0.0019
TSMC	0.0900	0.0212	0.0162	5.0867	3.3633	2.0167	0.0260	0.0109	0.0020
FTSMC	0.0700	0.0285	0.0122	6.9700	4.3767	2.2600	0.0700	0.0248	0.0034
FTSM-ANN	0.0600	0.0281	0.0128	6.8800	4.3367	2.2133	0.0672	0.0242	0.0032

Figures 36 to 37, shows the plots of comparative analysis of all methods for Sag score, VSLEI. For SS value, PI based methods found to better fit and for VSLEI, FTSMC is good.

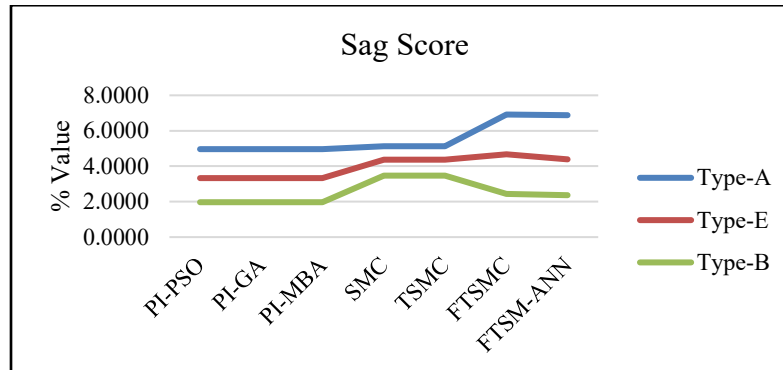


Figure 36. Plot of percent sag score.

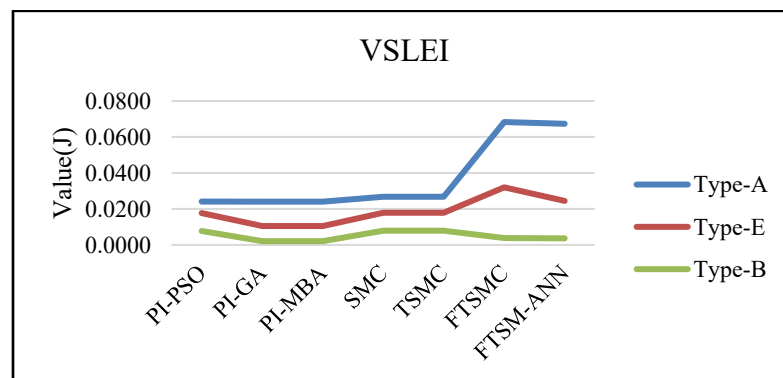


Figure 37. Plot of VSLEI.

6. Conclusion

This paper details the use of the dynamic voltage regulator to improve power quality, with a particular focus on the design of the controller. The proposed design procedure utilizes SMC concepts combined with nonlinear methods and ANN approach. The total voltage harmonic distortion and a per-unit change in supply voltage is measured through simulation to confirm the efficacy of the proposed mitigation strategy. After conducting comprehensive simulations for various types of voltage sags, a comparative analysis of control techniques based on quantitative measures such as HCR, SS, and VSLEI is performed. For all algorithms with all types of loads, the HCR value is close to 0. The variation in SS is from 45.14 to 4.96, for type-A, for type-B it is 29.22 to 1.97 and type-E value change is 14.74 to 2.08. Considering VSLEI, for Type-A, energy index varies from 24.69 to 0.0241, for type-B change is 2.0753 to 0.0019 and for Type-E variation is 9.9603 to 0.0105. Thus, significant improvement is found in both SS and VSLEI. The SS is improved by 80% and for VSLEI the increase is greater than 95%. The results showed that FTSMC combined with ANN is superior to other techniques for non-linear and combined load conditions, while the classical PI approach is more appropriate for linear load conditions. This suggested approach is versatile and can serve multiple purposes for effective compensation and power conditioning.

Conflict of Interest

The authors confirm that there is no conflict of interest to declare for this publication.

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AI Disclosure

During the preparation of this work the author(s) used generative AI in order to improve the language of the article. After using this tool/service, the author(s) reviewed and edited the content as needed and take(s) full responsibility for the content of the publication.

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